

THIS DRAWING AND SPECIFICATIONS, HEREIN, ARE THE PROPERTY OF INVENTEC CORPORATION AND SHALL NOT BE REPRODUCED, COPIED, OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION, INVENTEC CORPORATION, ALL RIGHT RESERVED.

NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

STRIX 2021 X60/SCAR

AMD CEZANNE-H + NV_GN20_E3/E5/E7

2020.09.24

21-OCT-2002		
DATE	CHANGE NO.	REV

DESIGN / DRAWER	XXX	DATE	21-OCT-2002
CHECK			
APPROVAL			
TITLE NAME			
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC			
MODEL,PROJECT,FUNCTION			
MAIN BOARD			
SIZE A3	CODE CS	DWG NUMBER 131000000-0-0	REV X01
SHEET #		119	

TABLE OF CONTENTS

RED:POWER
BLUE:APU
GREEN:GPU

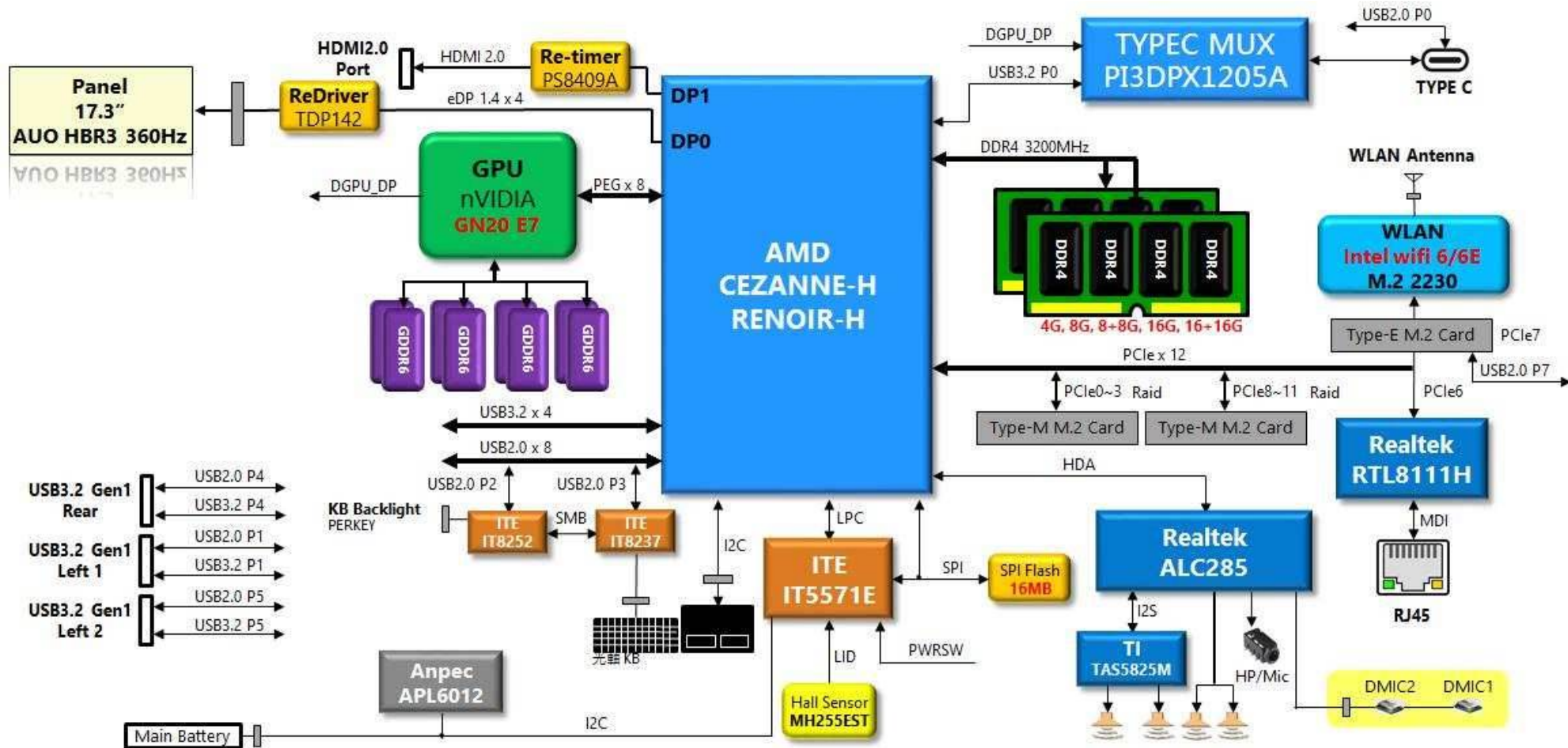
01.PROJECT NAME	41.AUDIO CODEC ALC285	79.GPU MEMORY FBA PARTITION 31-0
02.TABLE OF THE CONTENT	42.AUDIO AMP TAS5825M	80.GPU MEMORY FBA PARTITION 63-32
03.BLOCK DIAGRAM	43.AUDIO SPK/JACK	81.GPU MEMORY FBB PARTITION 31-0
04.POWER SEQUENCE	44.RESERVE	82.GPU MEMORY FBB PARTITION 63-32
05.HSIO MAP	45.M.2 FOR SSD1 (PCIE/SATA)	83.GPU MEMORY FBC PARTITION 31-0
06.SMBUS DIAGRAM	46.M.2 FOR SSD2 (PCIE/SATA)	84.GPU MEMORY FBC PARTITION 63-32
07.POWER BLOCK	47.LAN(RTL8111H)	85.GPU MEMORY FBD PARTITION 31-0
08.BATT/AC SHORT PROTECTION	48.RJ45 ESD TRANSFORMER	86.GPU MEMORY FBD PARTITION 63-32
09.DC IN	49.M.2 FOR WLAN/BT	87.GPU 27 MHZ XTAL
10.CHARGE (BQ24800)	50.RF CONN	88.GPU VBIOS, STRAPS
11.PD IN CHARGER(ISL9238)	51.EC IT5571E	89.GPU GPIO
12.P3V3AL_P5V0AL(RT6575B)	52.NKEY POWER	90.GPU IFP_AB
13.P12V0S(MPS_MP2263GD)	53.IT8237	91.GPU IFP_CD(DP)
14.P1V2_P0V6S (RT8231A)	54.NKEY IT8252E	92.GPU IFP_EF
15.P2V5 (RT8097A)	55.KB / EAGLE EYE RGB LED	93.OVR-M
16.P0V75 (SY8386R)	56.IT8013	94.GPU GND
17.P0V75S (SY8386R)	57.KB CNTR / TOUCH PAD	95.GPU POWER
18.P1V8A (SY8386R)	58.TPEC REDRIVER	96.GPU NVVDD DECOUPLING
19.ISL62776	59.USB TYPE-C PD TPS65993	97.GPU FBVDDQ DECOUPLING
20.PVCORE SIC634_1-2P	60.TYPE-C CNTR	98.GPU MSVDD DECOUPLING
21.PVCORE SIC634_3-4P	61.USB3 CNTR1	99.GPU POWER SEQUENCE
22.PVCORE_NB SIC534	62.USB3 CNTR2	100.GPU POWER DISCHARGE
23.POWER SEQUENCE (1/3)	63.USB3 CNTR3	101.GPU_NVVDD/NVVDDS (ON_NCP81610)
24.POWER SEQUENCE (2/3)	64.THERMAL / EC SHUTDOWN	102.PVCORE_DGPU (ON_NCP303150_1-2P)
25.POWER SEQUENCE (3/3)	65.THERMAL APL6012	103.PVCORE_DGPU (ON_NCP303150_3-4P)
26.FAN/HALL SENSOR	66.EMI	104.PVCORE_DGPU (ON_NCP303150_5-6P)
27.DDR4_DIMM0_CONN	67.RF	105.PVCORE_DGPU (ON_NCP303150_7P)
28.DDR4_DIMM1_CONN	68.DEBUG	106.P1V35S_DGPU (RT8816A_2P)
29.APU_FP6_MEMORY_CHA	69.(RESERVED)	107.P0V95S_DGPU (RT8068A)
30.APU_FP6_MEMORY_CHB	70.MB_NFC & USB2 CNTR4	108.P1V8S_AON1 (SY8386)
31.APU_FP6_DP/JTAG/TEST	71.MB_L.U/R.U-BAR/INDICATOR/MIC	109.PCBSCREW / MASK / STANDOFF
32.APU_FP6_I2C_AUDIO	GPU(GN20_E3/E5) PAGE 72-101	110.DB COVER
33.APU_FP6_LPC/SPI/XTAL/GPPCLK	72.GN20 E7	111.DB_LED L-U BAR
34.APU_FP6_PCIE/SATA	73.GN20 INFO	112.DB_LED R-U BAR
35.APU_FP6_USB	74.GPU PCI EXPRESS	113.DB_INDICATOR BOARD
36.APU_FP6_POWER	75.GPU MEMORY PARTITION A	114.DB_DMIC BOARD
37.APU_FP6_DGND	76.GPU MEMORY PARTITION B	115.DB_NFC CN, SW, LED
38.EDP_REDRIIVER/EDP CNTR	77.GPU MEMORY PARTITION C	116.DB_NFC IC
39.HDMI RETIMER PS8409A	78.GPU MEMORY PARTITION D	117.DB_PWRBTN
40.HDMI CONN		118.DB_HDT DEBUG
		119.POWER_SEQUENCE

INVENTEC

TITLE
MODEL PROJECT FUNCTION
TABLE OF THE CONTENT

CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	DOC NUMBER	1310xxxx-0-0	REV	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET	2	of	119				

G533Q/G733Q BLOCK DIAGRAM



BOM SKU CFG

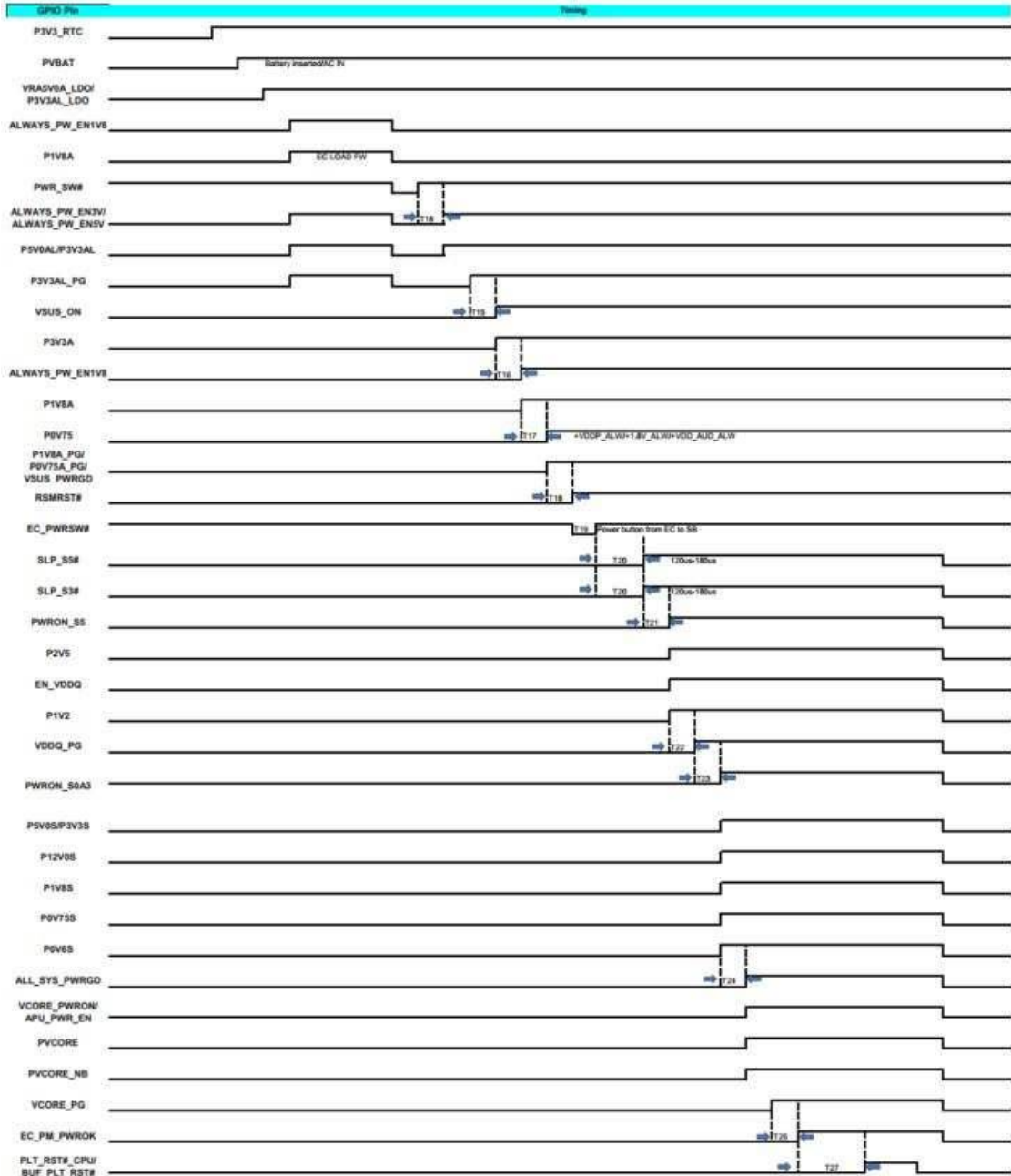
A:AMP
AC:AMP CODEC
P:PERKEY
Z:4ZONE BACKLIGHT
AP:PERKEY BACKLIGHT
AZ:NORMAL KEYBOARD
O:OPTICAL MECHANICAL

V:V-CUT LED
L:LOGO LED
N:NFC LED
K:KEY STONE
AA:MIC CN FOR 15"
AB:MIC CN FOR 17"

INVENTEC

CHANGE by		DATE	21-OCT-2002	SIZE	A3	CODE	CS	DOC NUMBER	1310xxxx-0-0	REV	X01
PCB P/N		PCB VER		SHEET		3		of 119			

POWER SEQUENCE



SIGNAL	VOTAGE	G3	S5	S3	S0	REMARK
P3V3AL_RTC	3.3V	O	O	O	O	COIN BATTERY
PVBAT	19V	X	O	O	O	DC-IN ALWAYS
P3V3AL	3.3V	X	O	O	O	DC-IN ALWAYS
P5V0AL	5V	X	O	O	O	DC-IN ALWAYS
P3V3A	3.3V	X	O	O	O	
P0V75A	0.75V	X	O	O	O	
P1V8A	1.8V	X	O	O	O	
P2V5	2.5V	X	X	O	O	
P1V2	1.2V	X	X	O	O	
P5V0S	5V	X	X	X	O	
P3V3S	3.3V	X	X	X	O	
P1V8S	1.8V	X	X	X	O	
P0V75S	0.75V	X	X	X	O	
P0V6S	0.6V	X	X	X	O	
PVCORE	SVC/SVD	X	X	X	O	
PVCORE_NB	SVC/SVD	X	X	X	O	

Table 42. Power Sequencing Group Definitions with Coin Cell Battery

Group	System Power Domain	Voltages
Group A	G3	VDDBT_RTC_G
Group B	S5	VDD_33_S5, VDD_18_S5, VDDIO_AUDIO, VDOP_S5,
	S3	VDDIO_MEM_S3
Group C	S0	VDD_33, VDD_18, VDDP: (Add delay (>1ms) between VDD_33 and VDD_18 ramp up power sequence).
Group D	S0	VDDCR_SOC, VDDCR_CPU** (AM4 only), VDDCR* (FP6 only)

www.teknisi-indonesia.com

INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE A3		DOC NUMBER 1310xxxx-0-0	
CODE CS		REV X01	
SHEET 4 of 119			

CHANGE by XXX

PCB P/N 60xxxxxxxxxx

DATE 21-OCT-2002

PCB VER XXX

SIZE A3

CODE CS

DOC NUMBER 1310xxxx-0-0

REV X01

SHEET 4 of 119

HSIO MAP

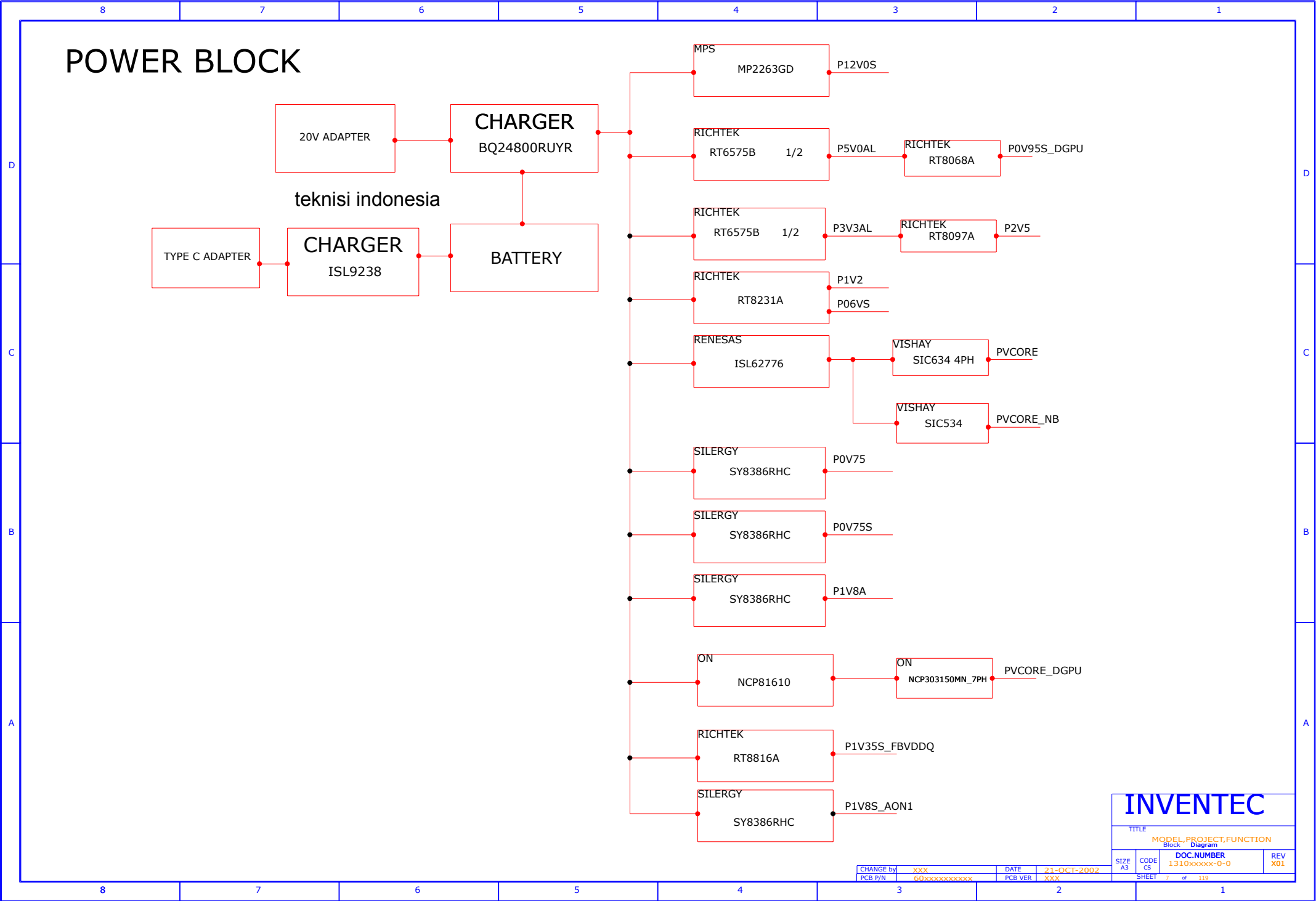
AMD Cezanne-H				
Mode		X60/SCAR	X50	AMD CRB
Display	DP0	eDP	eDP	eDP
	DP1	HDMI	HDMI	DP
USB 2.0	Port 0	TypeC	TypeC	TypeC
	Port 1	USB3 TypeA Left1	USB3 TypeA Left1	USB3 TypeA
	Port 2	IT8298	IT8298	USB2 TypeA
	Port 3	IT8237	NC	Camera
	Port 4	USB3 TypeA_REAR	USB3 TypeA_REAR	TypeC
	Port 5	USB3 TypeA Left2	USB3 TypeA Left2	USB3 TypeA
	Port 6	NC	NC	USB2 CN
	Port 7	Bluetooth	Bluetooth	USB2 CN
USB 3.0	Port 0	TypeC	TypeC	TypeC
	Port 1	USB3 TypeA Left1	USB3 TypeA Left1	USB3 TypeA
	Port 4	USB3 TypeA_REAR	USB3 TypeA_REAR	TypeC
	Port 5	USB3 TypeA Left2	USB3 TypeA Left2	USB3 TypeA
PEG X8	Port [0:7]	NV GN20 E3/E4/E5/E7	NV GN20 P0/P1	PCIE SLOT
PCIE	Port 0	PCIE SSD1	PCIE SSD1	SSD1
	Port 1			
	Port 2			
	Port 3			
	Port 4	NC	NC	SLOT
	Port 5	NC	NC	WWAN
	Port 6	Ethernet	Ethernet	Ethernet
	Port 7	WLAN	WLAN	WLAN
	Port 8	PCIE SSD2	PCIE SSD2	SSD2
	Port 9			
	Port 10			
	Port 11			
GPU	DP	GN20 E3/E4/E5/E7: IFPC	GN20 P0/P1: IFPE	

	Normal KB 4Zone+Func Key	Normal KB PerKey RGB+Func Key	Optical KB 4Zone+Func Key	Optical KB PerKey RGB+Func Key
IC	ITE	ITE	ITE	ITE
	IT8298 (ASUS: IT8299)	IT8298 (ASUS: IT8299)	IT8298 (ASUS: IT8299)	IT8298 (ASUS: IT8299)
功能	N-Key+ LED特效控制	N-Key+ LED特效控制	N-Key+ LED特效控制	N-Key+ LED特效控制
IC		ITE	ITE	ITE
		IT8013 (ASUS: IT8013)	IT8237 (ASUS: IT8237)	IT8237 (ASUS: IT8237)
功能		LED特效控制	N-KEY+ KB GPIO SCAN	N-KEY+ KB GPIO SCAN

CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	DOC NUMBER	1310xxxx-0-0	REV	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET	5	of	119				

INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram



INVENTEC

TITLE

MODEL, PROJECT, FUNCTION

Block Diagram

DOC. NUMBER

1310xxxx-0-0

REV

X01

CHANGE by

XXX

PCB P/N

60xxxxxxxxxx

DATE

21-OCT-2002

PCB VER

XXX

SIZE

A3

CODE

CS

SHEET

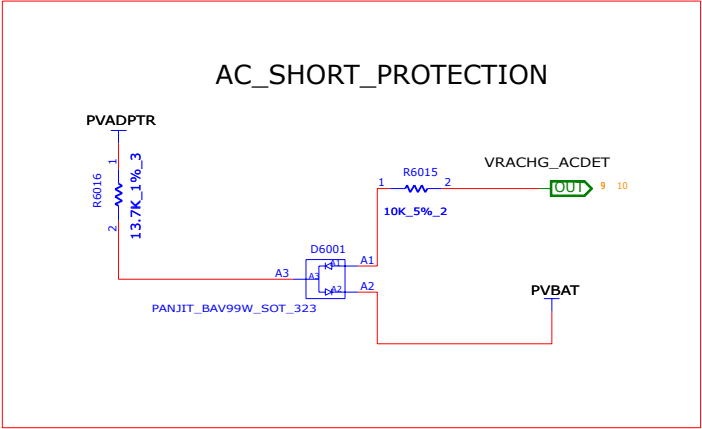
7

of

119

BATTERY / AC SHORT PROTECTION

LOCATION NUMBER : 6000~6999

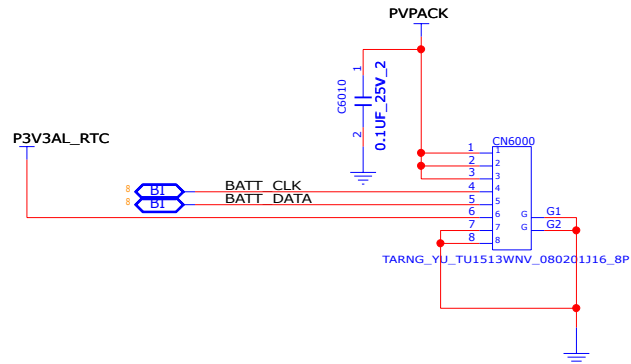
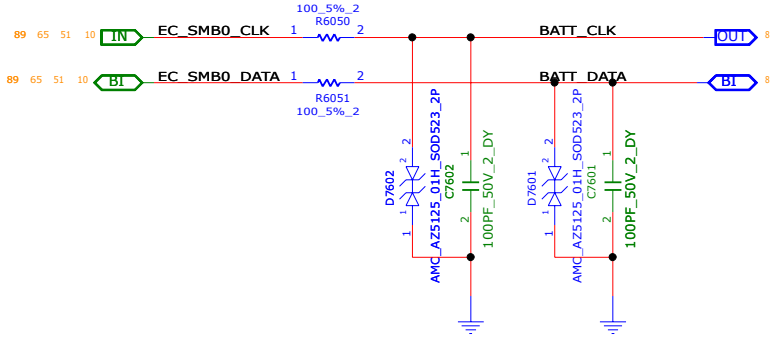


BATTERY PIN DEFINE

BATTERY SIDE		MAIN BOARD SIDE	
PIN1	P+	PIN1	P+
PIN2	P+	PIN2	P+
PIN3	SMBC	PIN3	P+
PIN4	SMBD	PIN4	SMBC
PIN5	RTC	PIN5	SMBD
PIN6	P-	PIN6	RTC
PIN7	P-	PIN7	P-
		PIN8	P-

BATT

I2C ADDR W/R 0XFE/0XFF



INVENTEC

TITLE

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE

A3

CODE

CS

SHEET

8 of 119

DOC.NUMBER

1310xxxx-0-0

REV

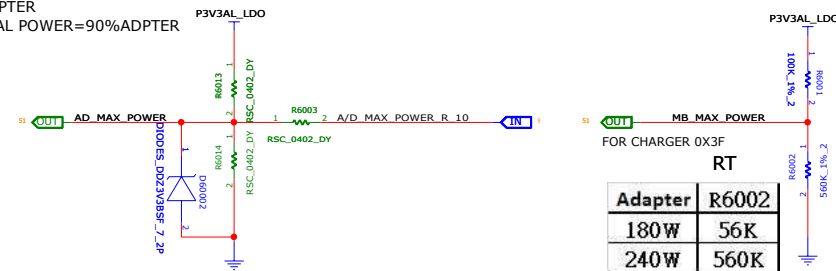
X01

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

DC_IN

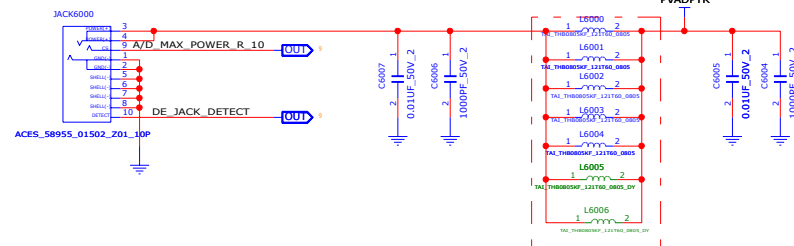
LOCATION NUMBER : 6000~6999

ADAPTER
TOTAL POWER=90%ADPTEP



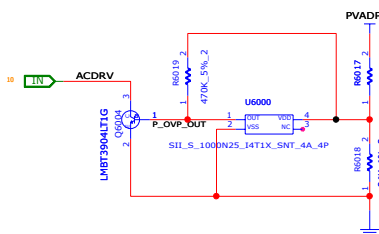
240W
12A

$6A \times 5 \times 0.7 = 21A > 12A$

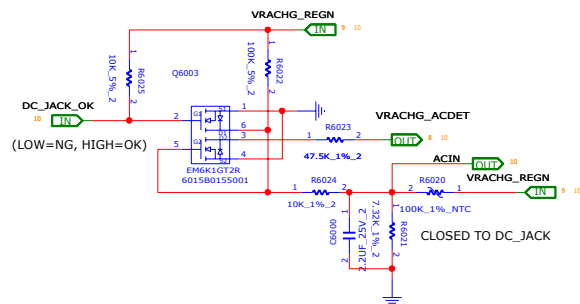


	N_SERIES	G_SERIES
RT	10MOHM	5MOHM
14K	0.4V	45W
31.6K	0.8V	150W
56K	1.2V	180W
93.1K	1.6V	65W
150K	2V	N/A
270K	2.4V	90W
560K	2.8V	120W

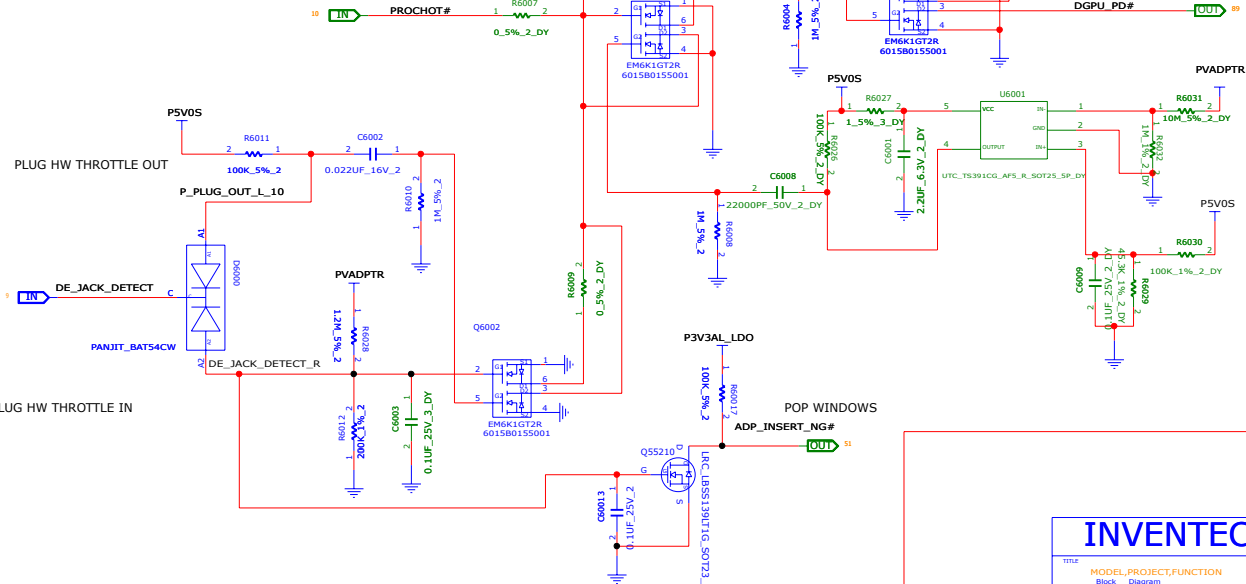
ADP_OVP_24V



DC_JACK_PROTECTION
DC JACK OT 95°C TEMP



AC LIMIT = 100% ADP
BAT LIMIT = BYTE 7 X 1.7



INVENTEC

TITLE			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A1	CS	1310xxxx-0-0	X01
SHEET			
1 of 110			

LOCATION NUMBER : 60000~60099



				TITLE MODEL,PROJECT,FUNCTION Block Diagram			
CHANGE BY		XXX	DATE		21-OCT-2002		
PCB P/N		60000000000000000000		PCB VER		XXX	
				SIZE A3		CODE CS	DOC NUMBER 1-01000000-030
				SHEET		35 of 110	
				REV		X01	

07e409180c100f00520f7a8d74001513

D



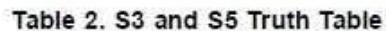
B

A

07e409180c100f00520f7a8d74001513

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 11 of 119			

LOCATION NUMBER : 60300~60399



STATE	S3	S5	VDDQ	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

INVENTEC

TITLE

MODEL, PROJECT, FUNCTION

SIZE	CODE	DOC.NUMBER
12	12	1310xxxxx-0-0

REV
X01

CHANGE by	XXX
PCB P/N	60XXXXXXXXXX

DATE	21-OCT-2002
PCB VER	XXX

	SIZE	
	A3	
		S

CODE
CS 1310xxx

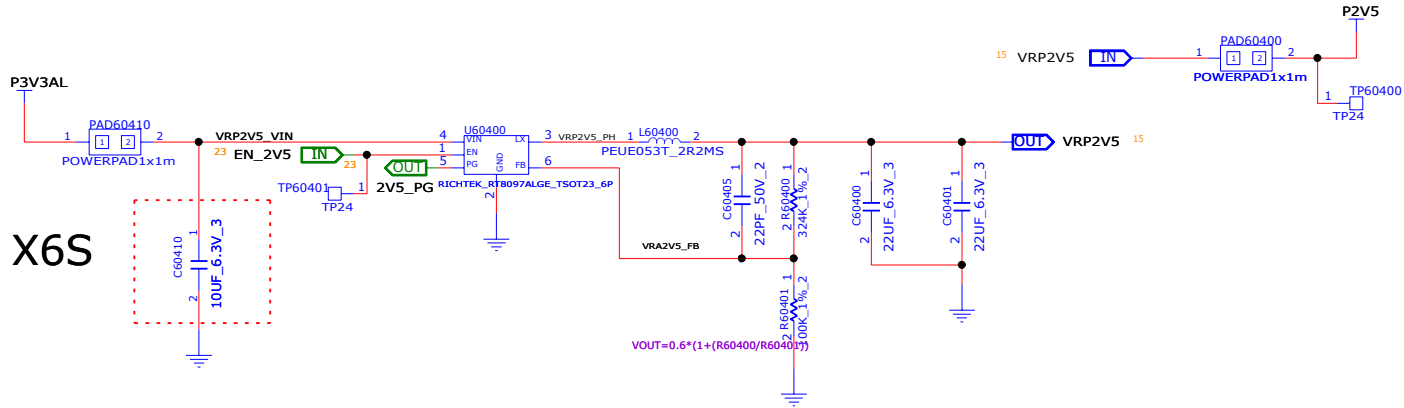
SHEET 14 of 116

X01

P2V5 (RT8097A)

LOCATION NUMBER : 60400~60499

www.teknisi-indonesia.com



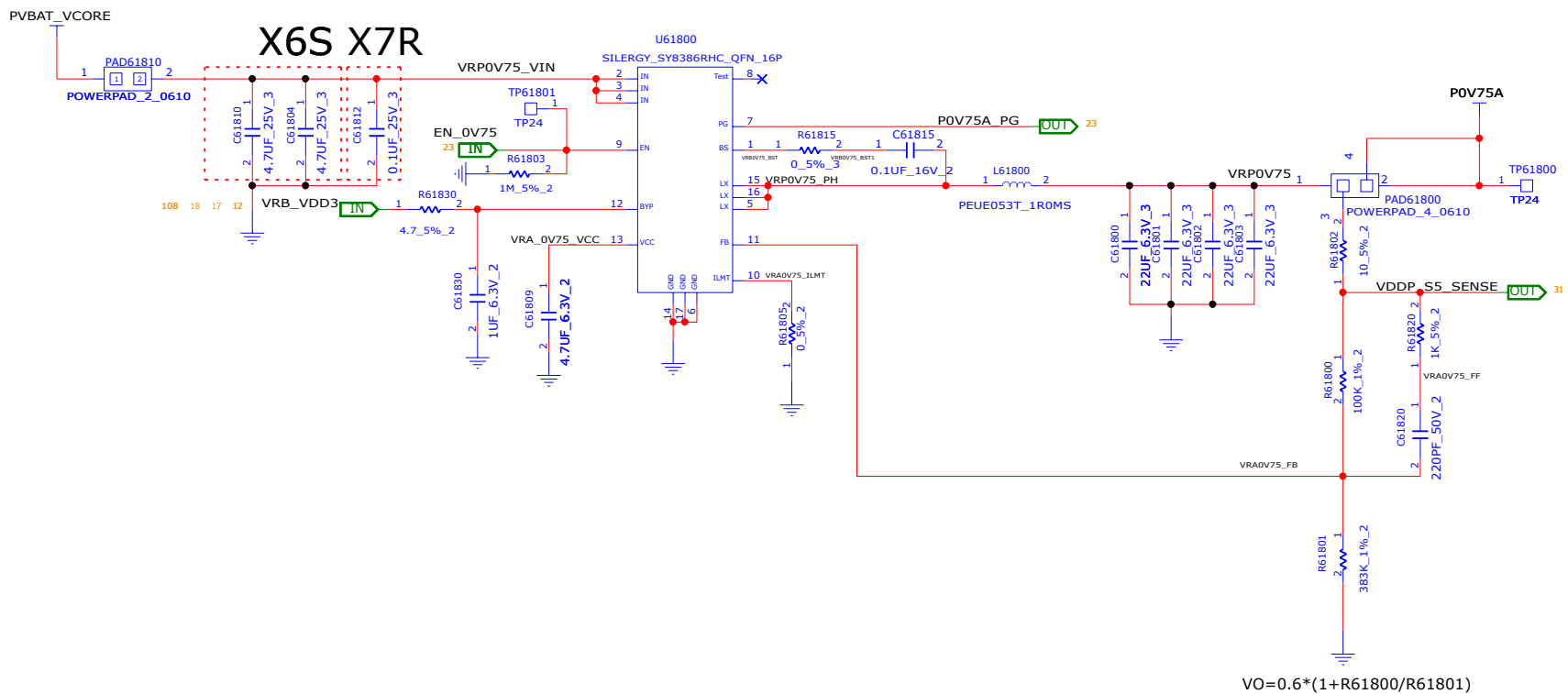
INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
P2V5			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 15 of 119			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX
3		2	

P0V75 (SY8386R)

LOCATION NUMBER : 61800~61849



$$VO=0.6*(1+R61800/R61801)$$

INVENTEC

TITLE

MODEL, PROJECT, FUNCTION

Block Diagram

DOC. NUMBER

1310xxxx-0-0

REV

X01

CHANGE by

XXX

DATE

21-OCT-2002

PCB P/N

60xxxxxxxxxx

PCB VER

XXX

SIZE

A3

CODE

CS

SHEET

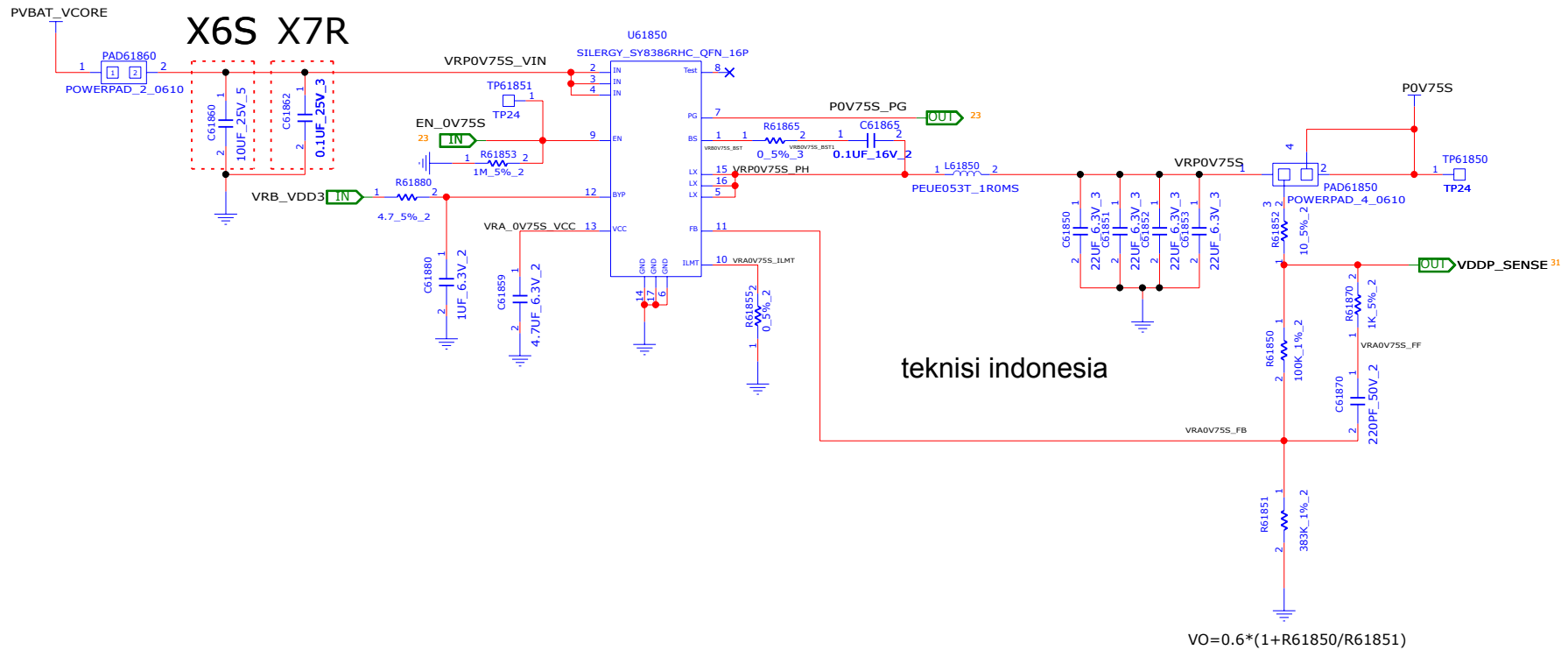
16

of

119

P0V75S (SY8386R)

LOCATION NUMBER : 61850~61899



teknisi indonesia

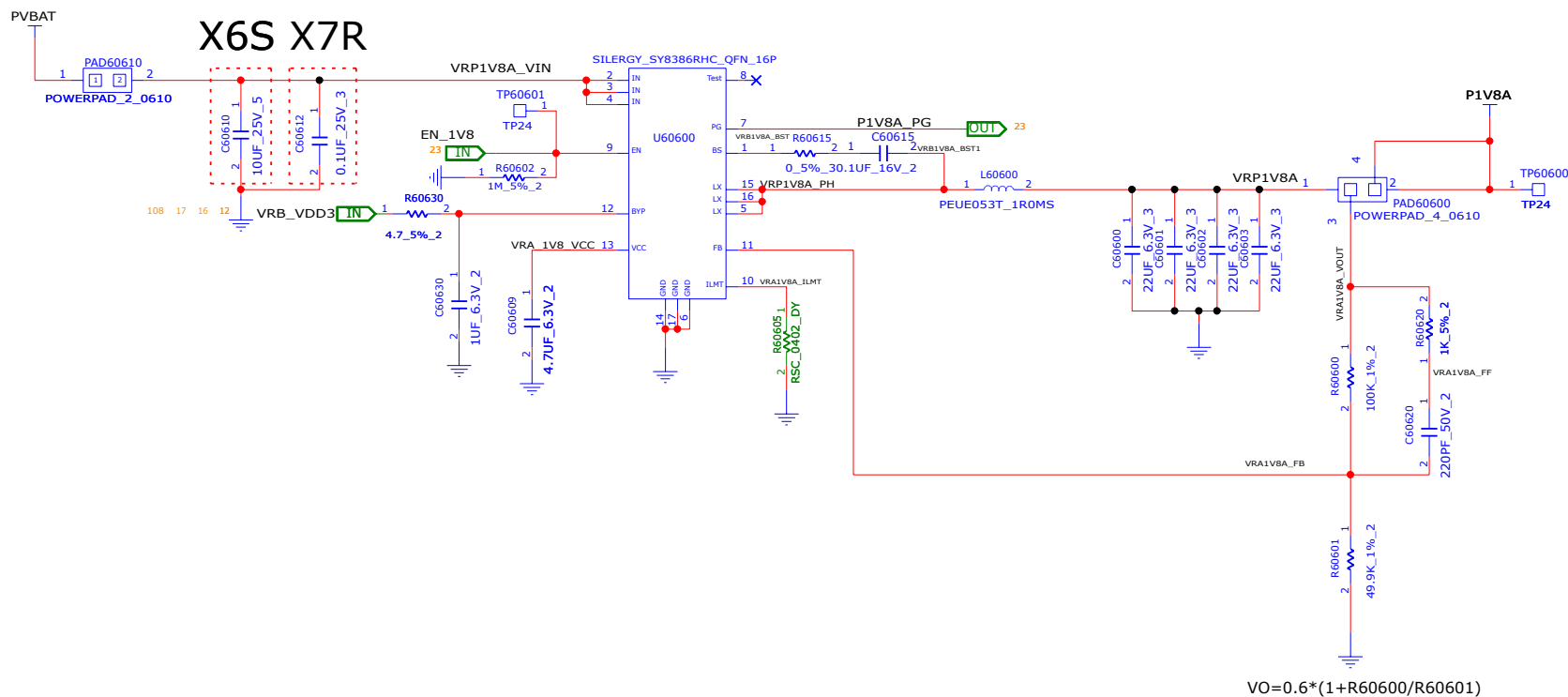
INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET	17	of 119	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

P1V8A (SY8386R)

LOCATION NUMBER : 60600~60699



$$VO = 0.6 * (1 + R60600 / R60601)$$

INVENTEC

TITLE

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE	CODE	DOC. NUMBER
13	00	1310xxxxx-0-0

REV
X01

CHANGE by	xxx
PCB P/N	60xxxxxxxxxxx

DATE	21-OCT-2002
PCB VER	XXX

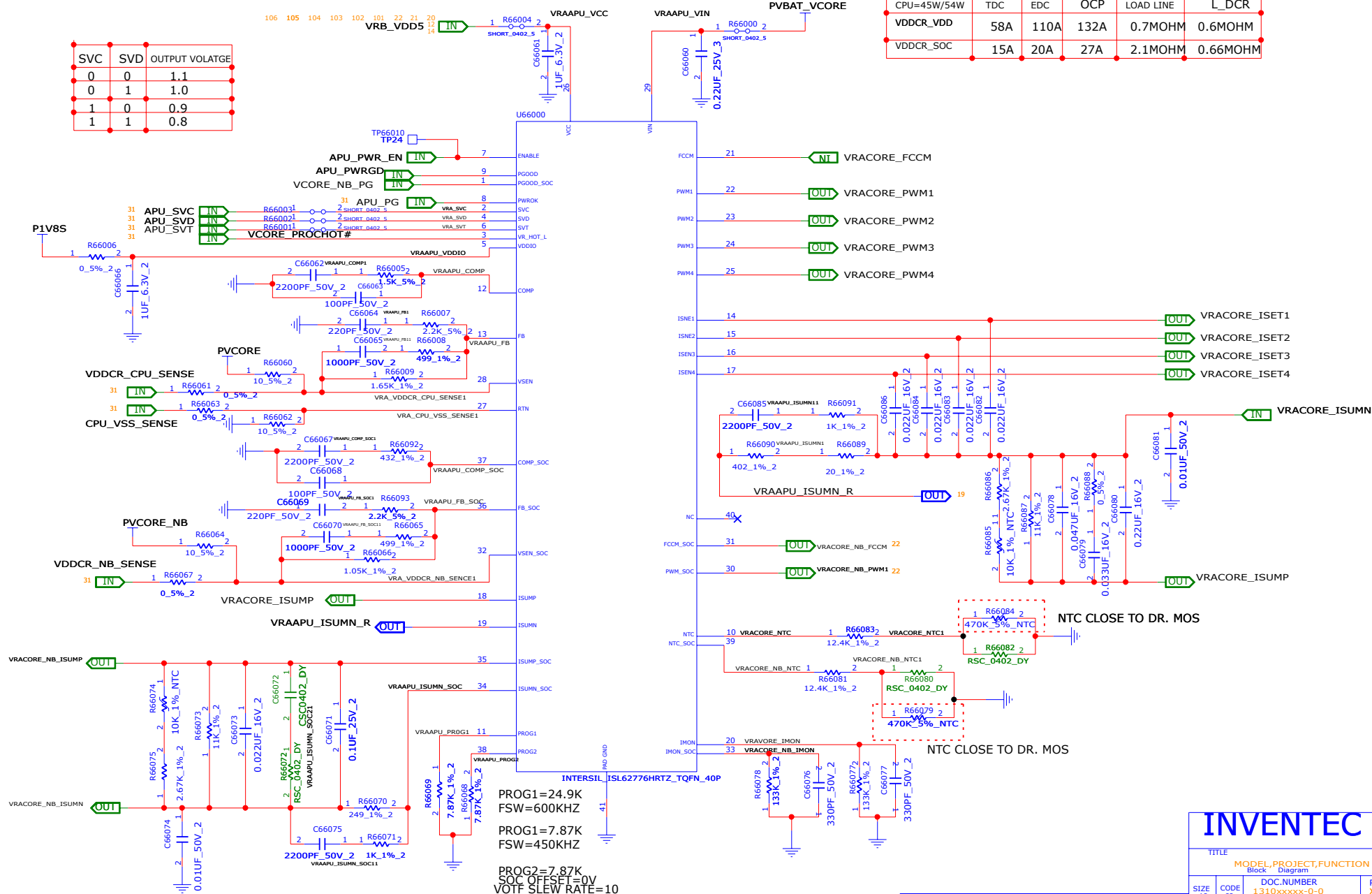
SIZE A3	CODE CS	1310xxxx
SHEET		18 of 116

	X01
--	-----

LOCATION NUMBER : 66000~66999

SVC	SVD	OUTPUT VOLATGE
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

CPU=45W/54W	TDC	EDC	OCP	LOAD LINE	L_DCR
VDDCR_VDD	58A	110A	132A	0.7MOHM	0.6MOHM
VDDCR_SOC	15A	20A	27A	2.1MOHM	0.66MOHM



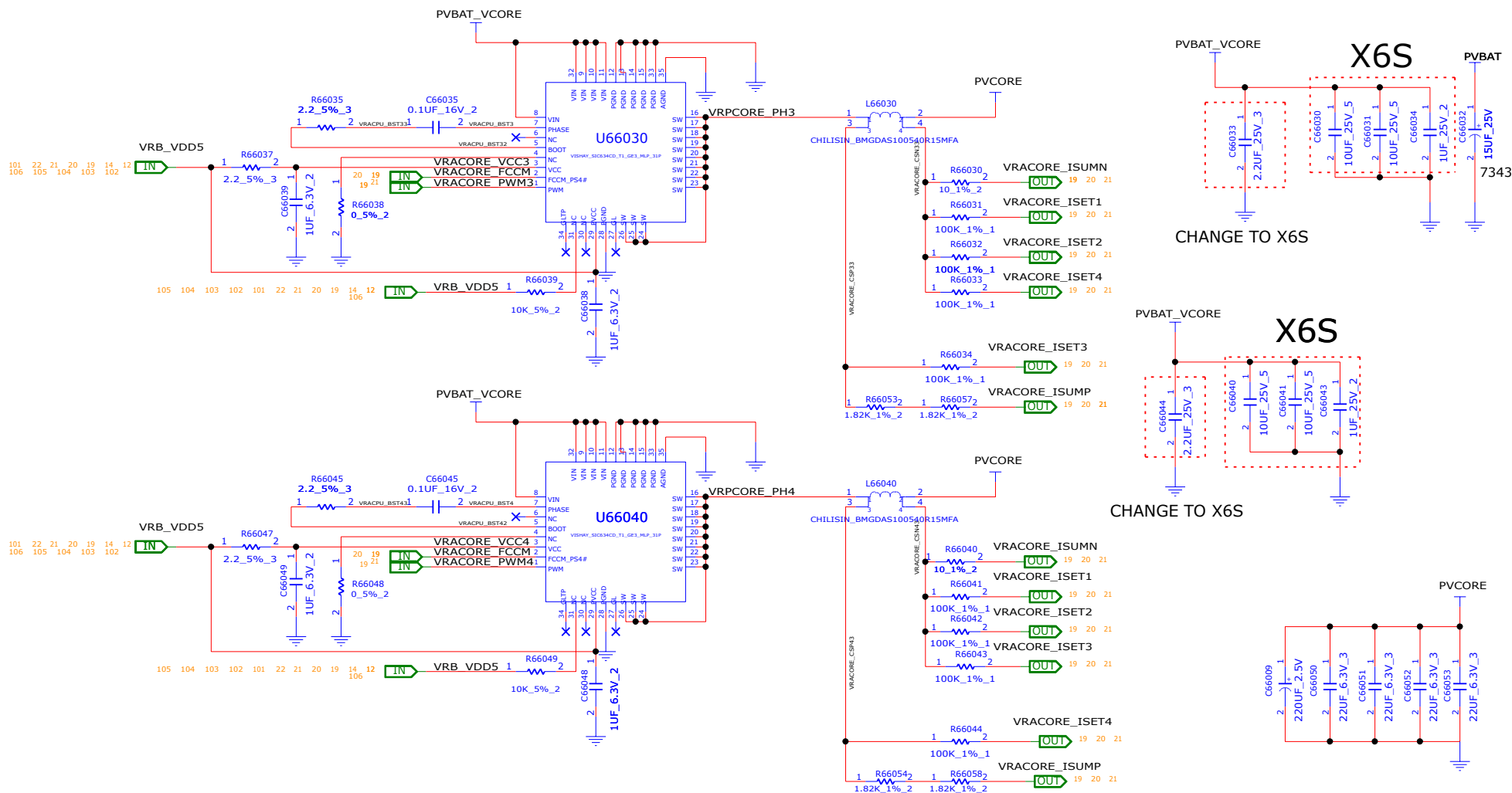
INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
		Block	Diagram
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxxx-0-0	REV X01
SHEET		19 of 119	

CHANGE by	xxx	DATE	21-OCT-200
PCB P/N	60xxxxxxxxxxx	PCB VER	xxx

07e409180c100f00520f7a8d74001513

LOCATION NUMBER : 66000~66999



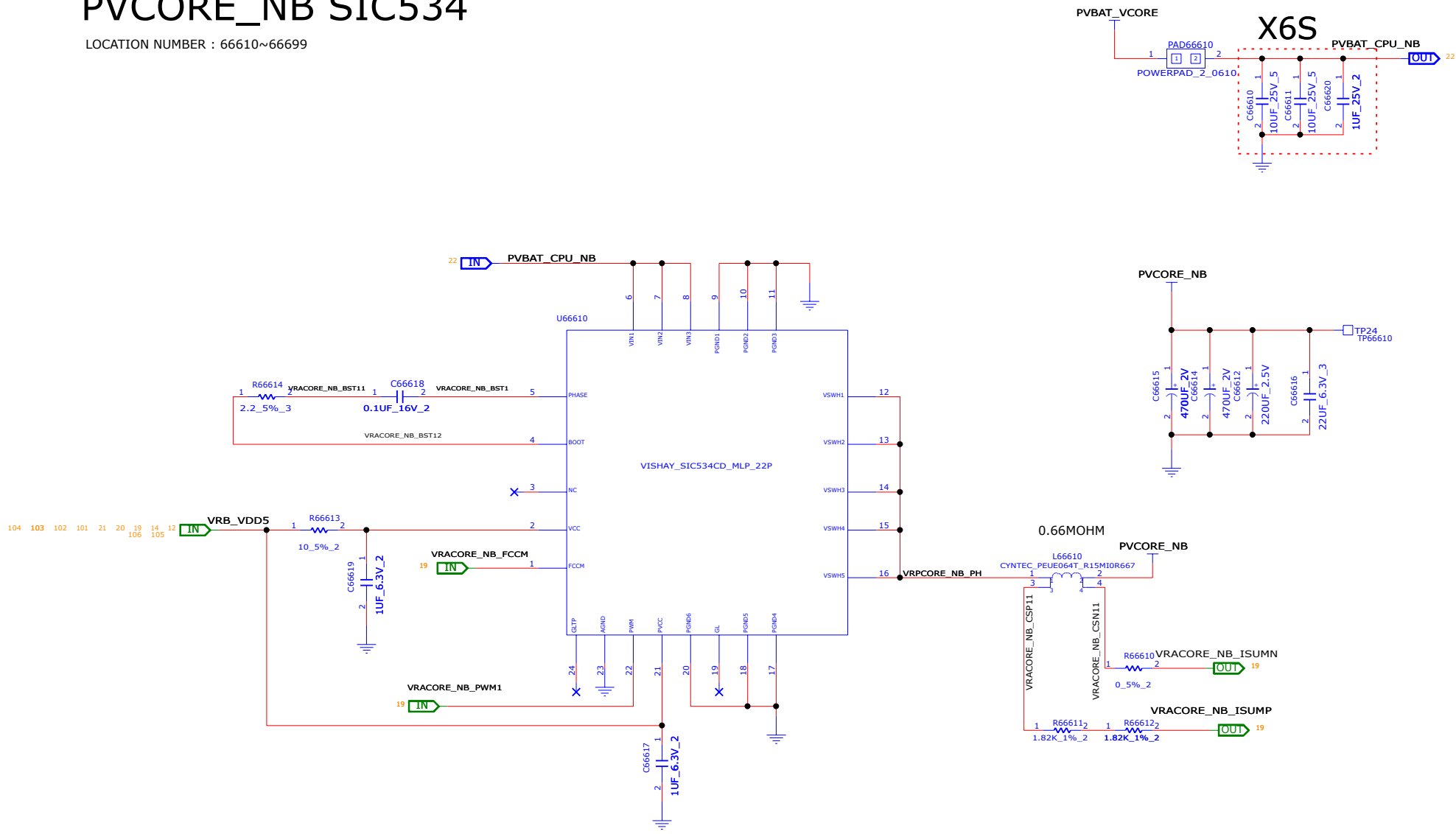
INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
		Block	Diagram
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxxx-0-0	REV X01
SHEET		21 of 119	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

PVCORE_NB SIC534

LOCATION NUMBER : 66610~66699



INVENTEC

TITLE

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE

A3

CODE

CS

SHEET

22 of 119

DOC.NUMBER

1310xxxx-0-0

REV

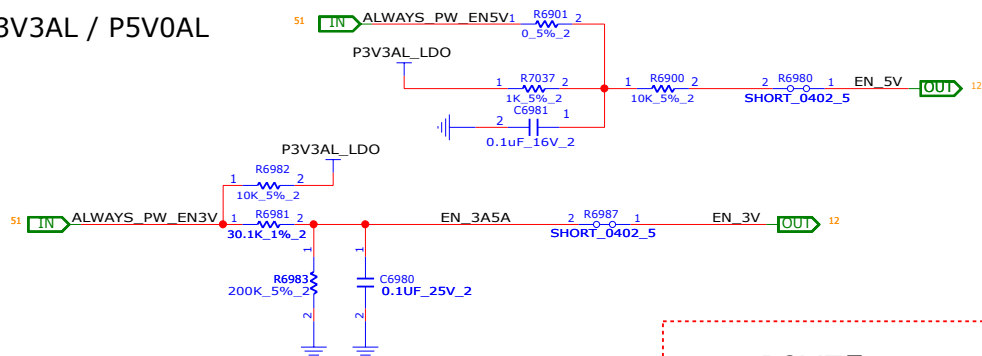
X01

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

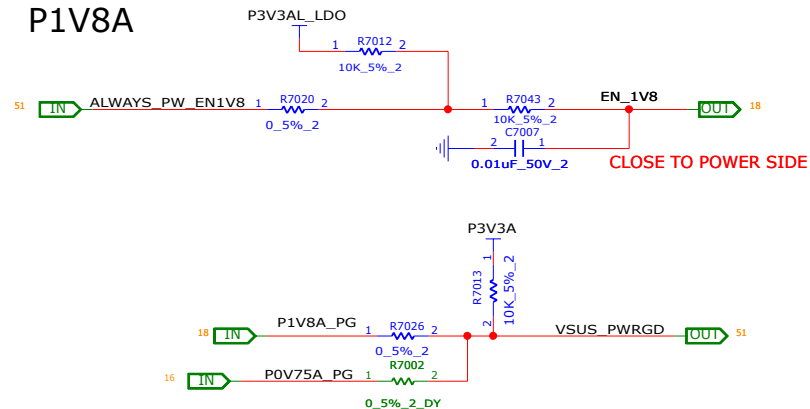
POWER SEQUENCE (1/3)

LOCATION NUMBER : 6900~7099

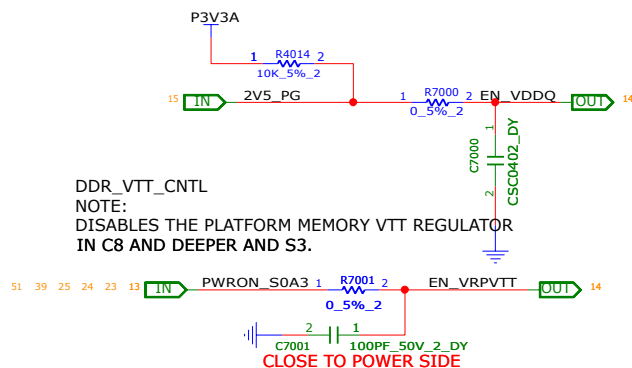
P3V3AL / P5V0AL



P1V8A



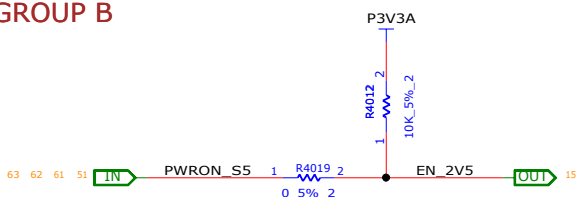
DDR4 P1V2/VTT/VPP



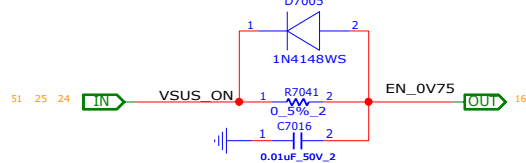
DDR_VTT_CNTL

NOTE:
DISABLES THE PLATFORM MEMORY VTT REGULATOR
IN C8 AND DEEPER AND S3.

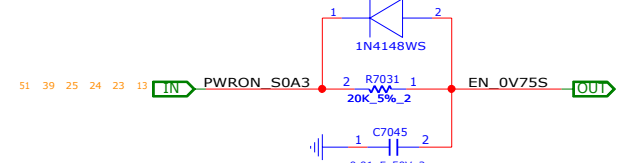
GROUP B



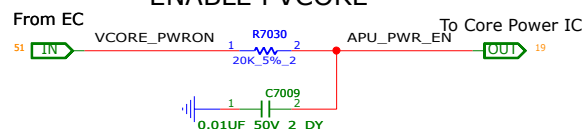
P0V75



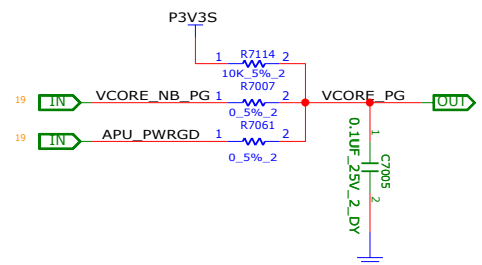
P0V75S



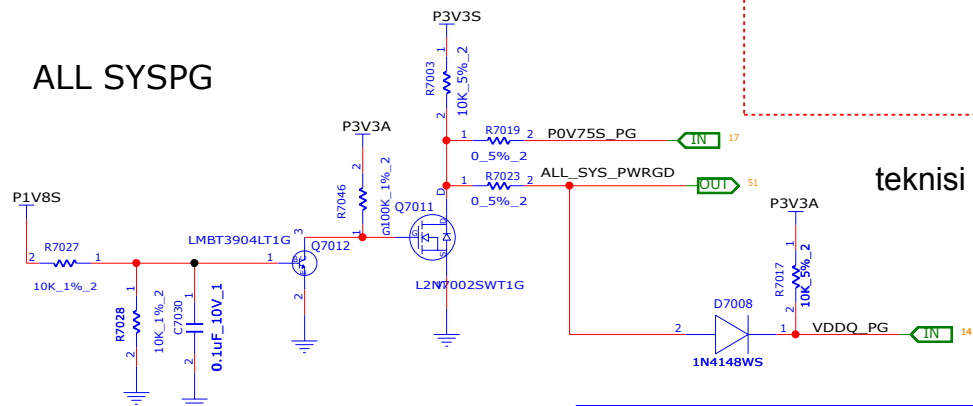
ENABLE PVCORE



CPU VCORE PWRGD



ALL SYSPG



teknisi indonesia

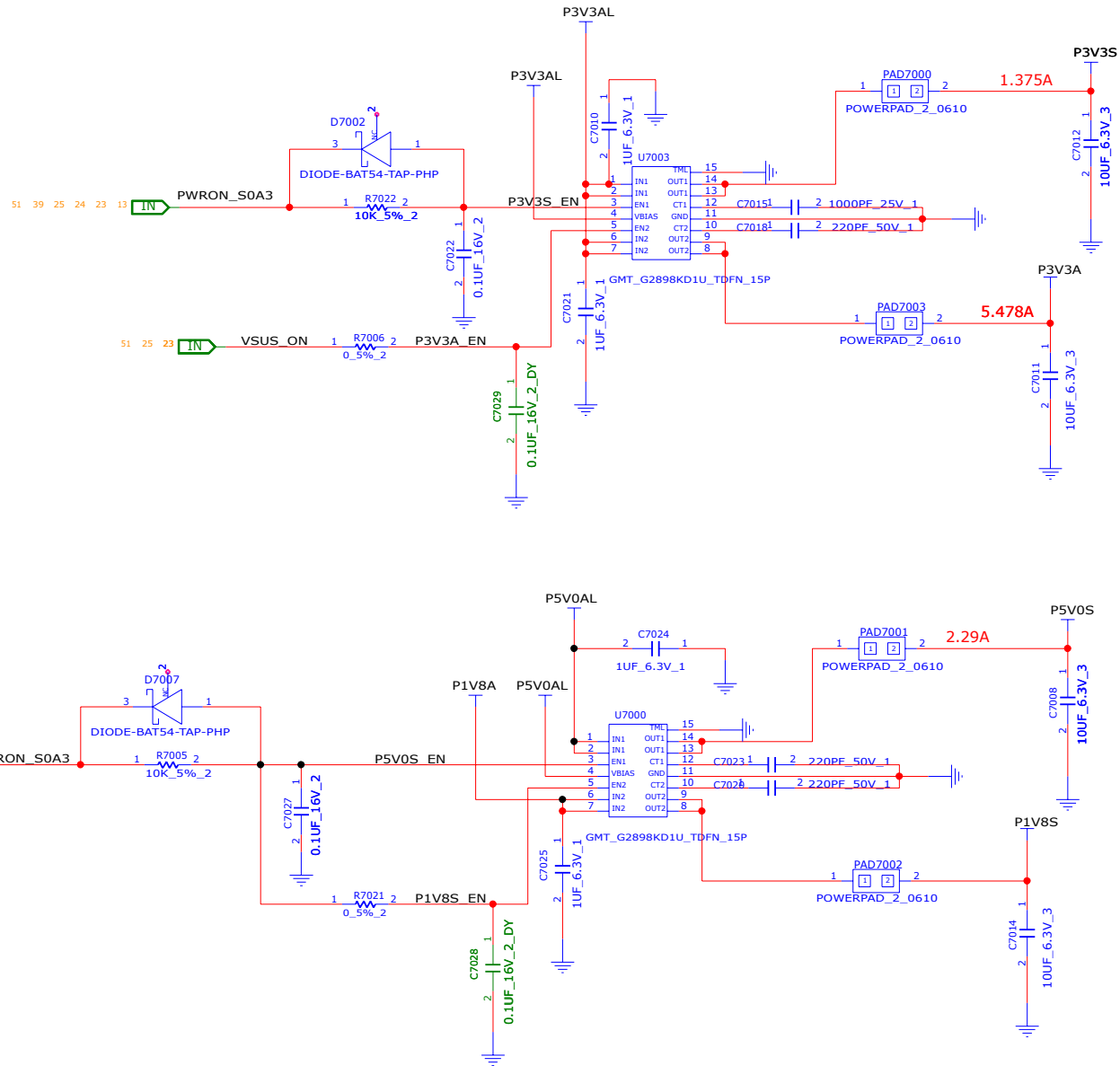
INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		23 of 119	

CHANGE by	xxx	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	xxx

POWER SEQUENCE (2/3)

LOCATION NUMBER : 7000~7099

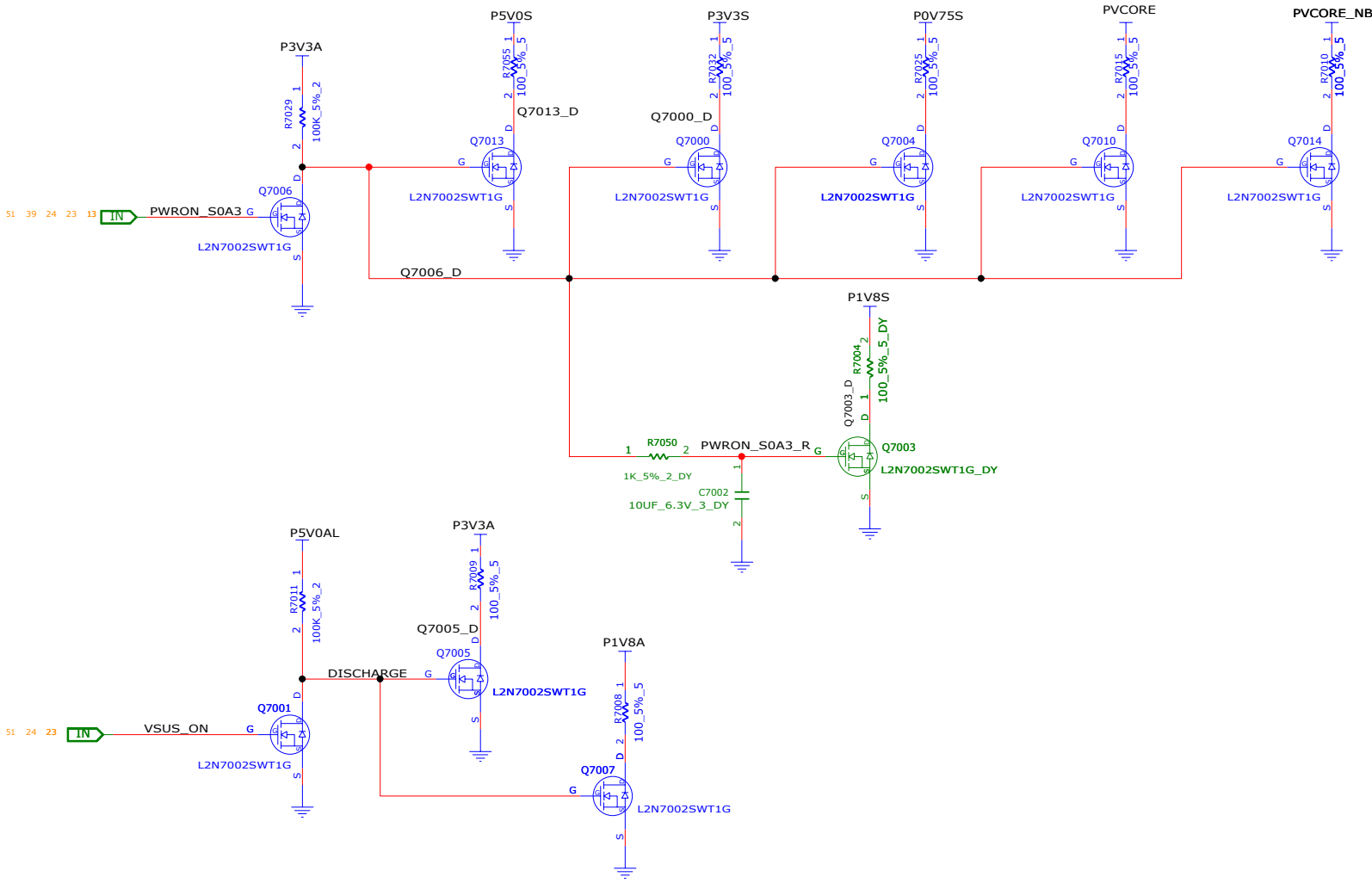
**INVENTEC**

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET	24	of 119	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

POWER SEQUENCE (3/3)

LOCATION NUMBER : 7000~7099



INVENTEC

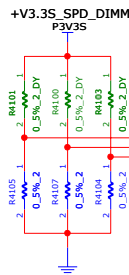
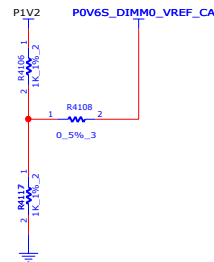
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET		25 of 119	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

DDR4_DIMM0_CONN

LOCATION NUMBER : 4100~4199(DDR)

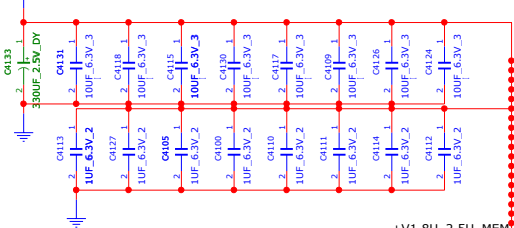
CHA H=4.0MM



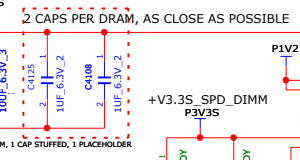
NOTE:
[SA2 SA1 SA0]=[0 0 0]

SA0 DIMM0
SA1 DIMM0
SA2 DIMM0

+VDD2_MEM P1V2 PLACE THE DISCRETES CLOSE TO SODIMM AND DISTRIBUTE EVENLY ON EACH SIDE OF THE DIMM



+V_VDD2_VTT P0V6S



2 CAPS PER DRAM, AS CLOSE AS POSSIBLE

PLACED ON VTT PLANE CLOSE TO DIMM, 1 CAP STUFFED, 1 PLACEHOLDER

+V3.3S_SPD_DIMM P3V3S

2.2UF 6.3V 2.DY
0.1UF 25V 2.DY

+VREF_CH0_CA P0V6S_DIMM0_VREF_CA

0.1UF 10V 1
2.2UF 6.3V 1

+V1.8U_2.5U_MEM P2V5

2.2UF 6.3V 2.DY
0.1UF 25V 2.DY

M_A_EVENT#
M_A_RST#
M_A_ACT#
M_A_ALERT#
M_A_PARITY

M_A_EVENT#
M_A_RST#
M_A_ACT#
M_A_ALERT#
M_A_PARITY

M_A_EVENT#
M_A_RST#
M_A_ACT#
M_A_ALERT#
M_A_PARITY

M_A_EVENT#
M_A_RST#
M_A_ACT#
M_A_ALERT#
M_A_PARITY

M_A_EVENT#
M_A_RST#
M_A_ACT#
M_A_ALERT#
M_A_PARITY

M_A_EVENT#
M_A_RST#
M_A_ACT#
M_A_ALERT#
M_A_PARITY

M_A_EVENT#
M_A_RST#
M_A_ACT#
M_A_ALERT#
M_A_PARITY

M_A_EVENT#
M_A_RST#
M_A_ACT#
M_A_ALERT#
M_A_PARITY

M_A_EVENT#
M_A_RST#
M_A_ACT#
M_A_ALERT#
M_A_PARITY

M_A_EVENT#
M_A_RST#
M_A_ACT#
M_A_ALERT#
M_A_PARITY

M_A_EVENT#
M_A_RST#
M_A_ACT#
M_A_ALERT#
M_A_PARITY

M_A_EVENT#
M_A_RST#
M_A_ACT#
M_A_ALERT#
M_A_PARITY

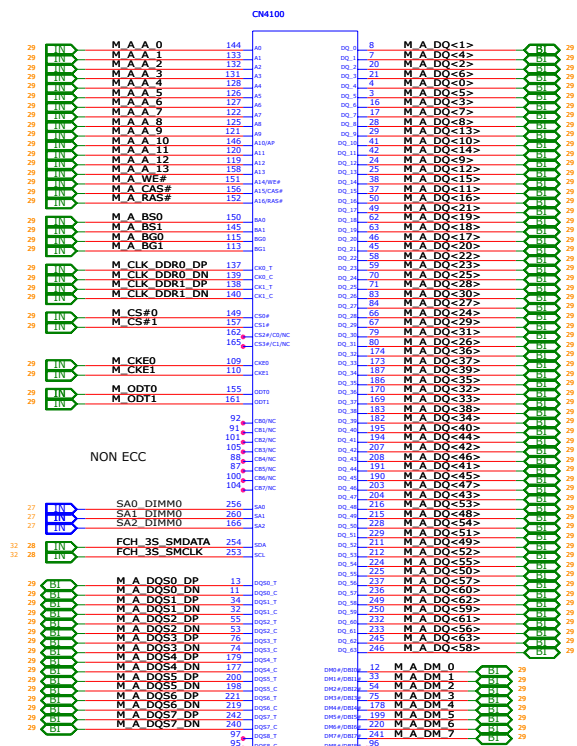
M_A_EVENT#
M_A_RST#
M_A_ACT#
M_A_ALERT#
M_A_PARITY

M_A_EVENT#
M_A_RST#
M_A_ACT#
M_A_ALERT#
M_A_PARITY

M_A_EVENT#
M_A_RST#
M_A_ACT#
M_A_ALERT#
M_A_PARITY

M_A_EVENT#
M_A_RST#
M_A_ACT#
M_A_ALERT#
M_A_PARITY

M_A_EVENT#
M_A_RST#
M_A_ACT#
M_A_ALERT#
M_A_PARITY



NON ECC

SA0 DIMM0
SA1 DIMM0
SA2 DIMM0

FCH_3S_SMDATA
FCH_3S_SMCLK

M_A_DOS0_DP
M_A_DOS0_DN
M_A_DOS1_DP
M_A_DOS1_DN
M_A_DOS2_DP
M_A_DOS2_DN
M_A_DOS3_DP
M_A_DOS3_DN
M_A_DOS4_DP
M_A_DOS4_DN
M_A_DOS5_DP
M_A_DOS5_DN
M_A_DOS6_DP
M_A_DOS6_DN
M_A_DOS7_DP
M_A_DOS7_DN

M_A_DM0
M_A_DM1
M_A_DM2
M_A_DM3
M_A_DM4
M_A_DM5
M_A_DM6
M_A_DM7

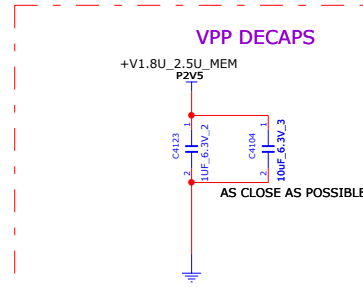
M_A_DM0
M_A_DM1
M_A_DM2
M_A_DM3
M_A_DM4
M_A_DM5
M_A_DM6
M_A_DM7

M_A_DM0
M_A_DM1
M_A_DM2
M_A_DM3
M_A_DM4
M_A_DM5
M_A_DM6
M_A_DM7

M_A_DM0
M_A_DM1
M_A_DM2
M_A_DM3
M_A_DM4
M_A_DM5
M_A_DM6
M_A_DM7

M_A_DM0
M_A_DM1
M_A_DM2
M_A_DM3
M_A_DM4
M_A_DM5
M_A_DM6
M_A_DM7

X50:6026B0328101
X60:6026B0456501



AS CLOSE AS POSSIBLE

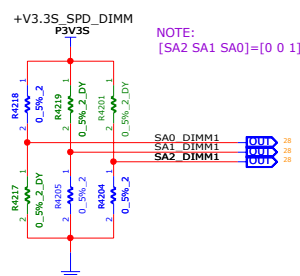
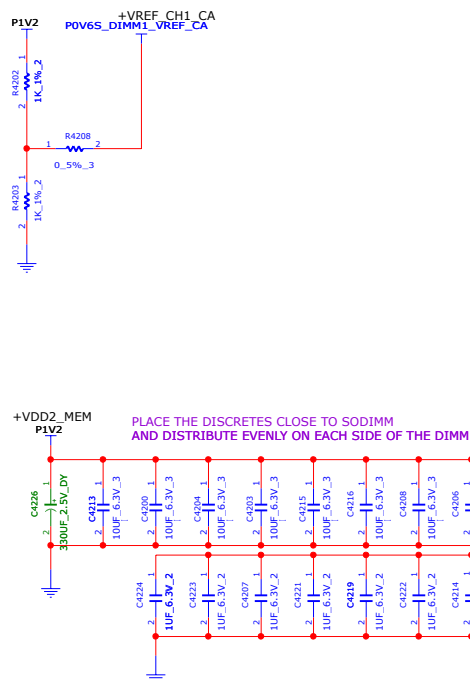
REFERENCE NUMBER:4100~4199

INVENTEC

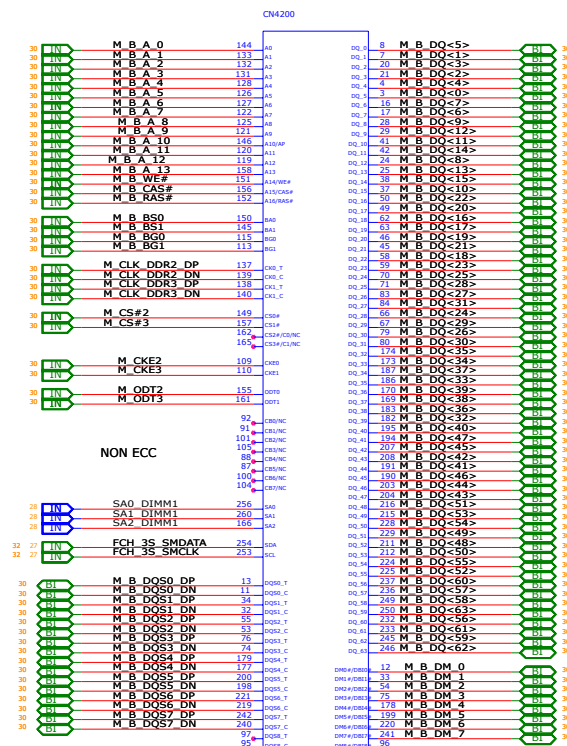
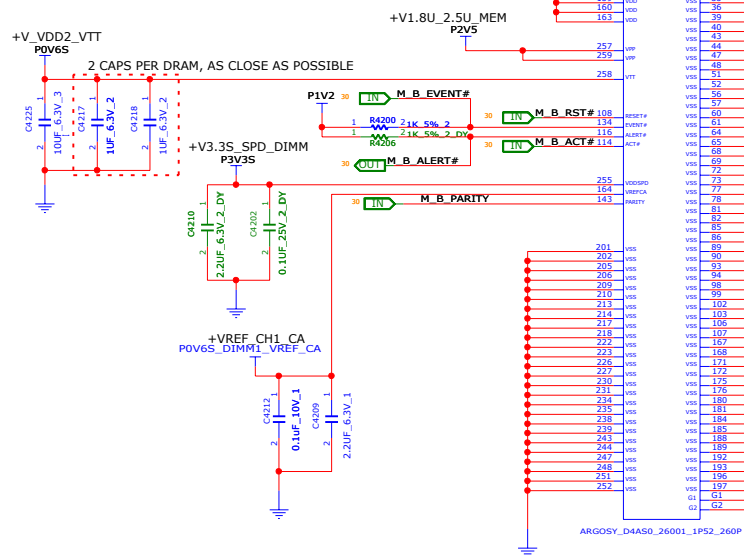
CHANGE BY	DATE	21-OCT-2002
PCB P/N	PCB VER	XXX
SIZE A1	CODE CS	1310xxxx-0-0
SHEET	REV	110

LOCATION NUMBER : 4200~4299(DDR)

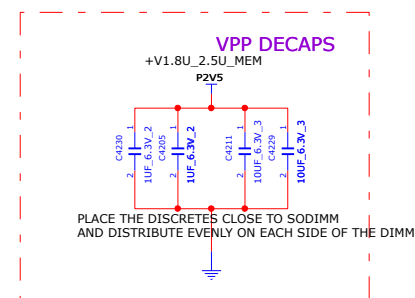
Diagram 2: A circuit diagram showing a voltage divider. A 1kV2 source is connected to a 1K 1% 2 resistor (R4202). The other end of R4202 is connected to a node. This node is also connected to a 1K 1% 2 resistor (R4203) which is connected to ground. A 0.5%_3 resistor (R4208) is connected between the node and the +VREF CH1_CA input of the P0V6S_DIMM1_VREF_CA pin.



NOTE:
[SA2 SA1 SA0]=[0 0 1]



X50:6026B0328201
X60:6026B0363901

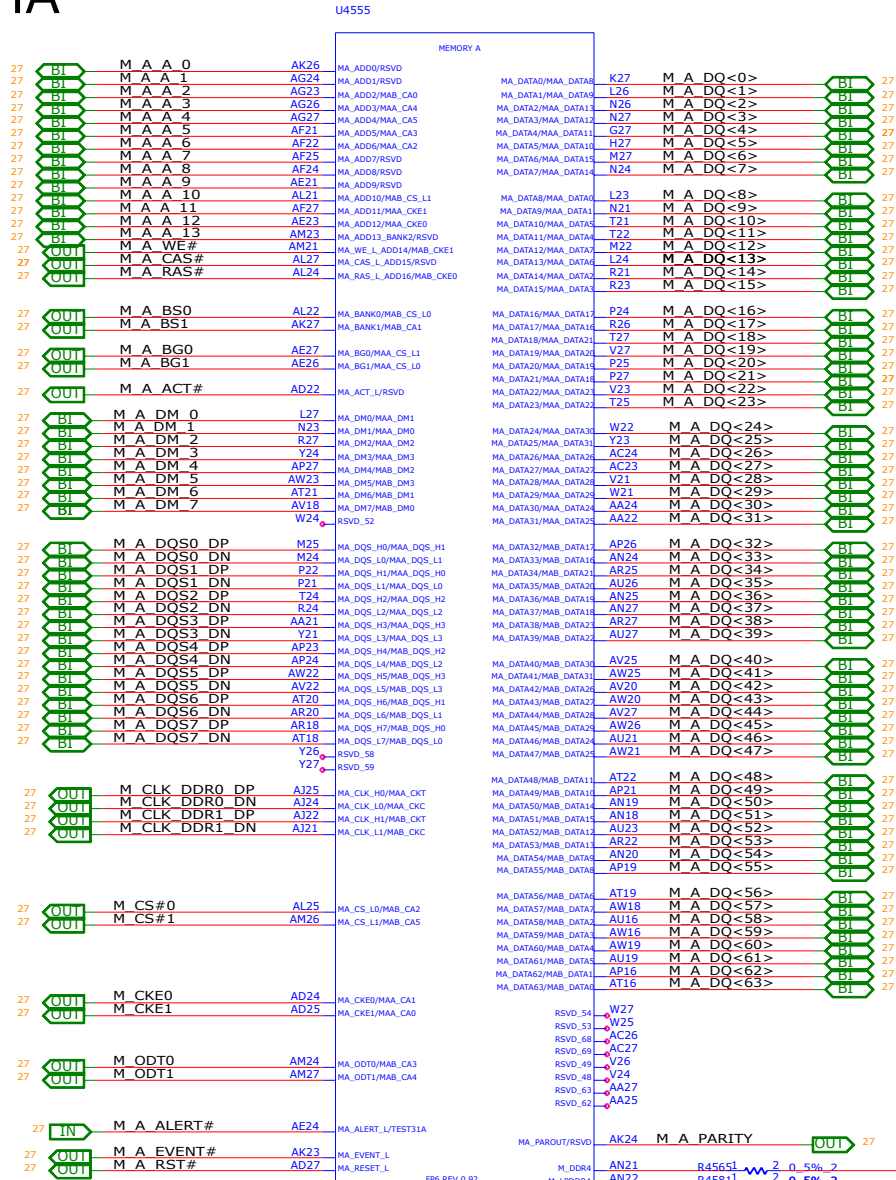


INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block		Diagram	
SIZE A3	CODE CS	DOC. NUMBER 1310xxxxxx-0-0	REV X01
SHEET		28 of 119	

APU_FP6_MEMORY CHA

LOCATION NUMBER : 4500~4999(APU)



INVENTEC

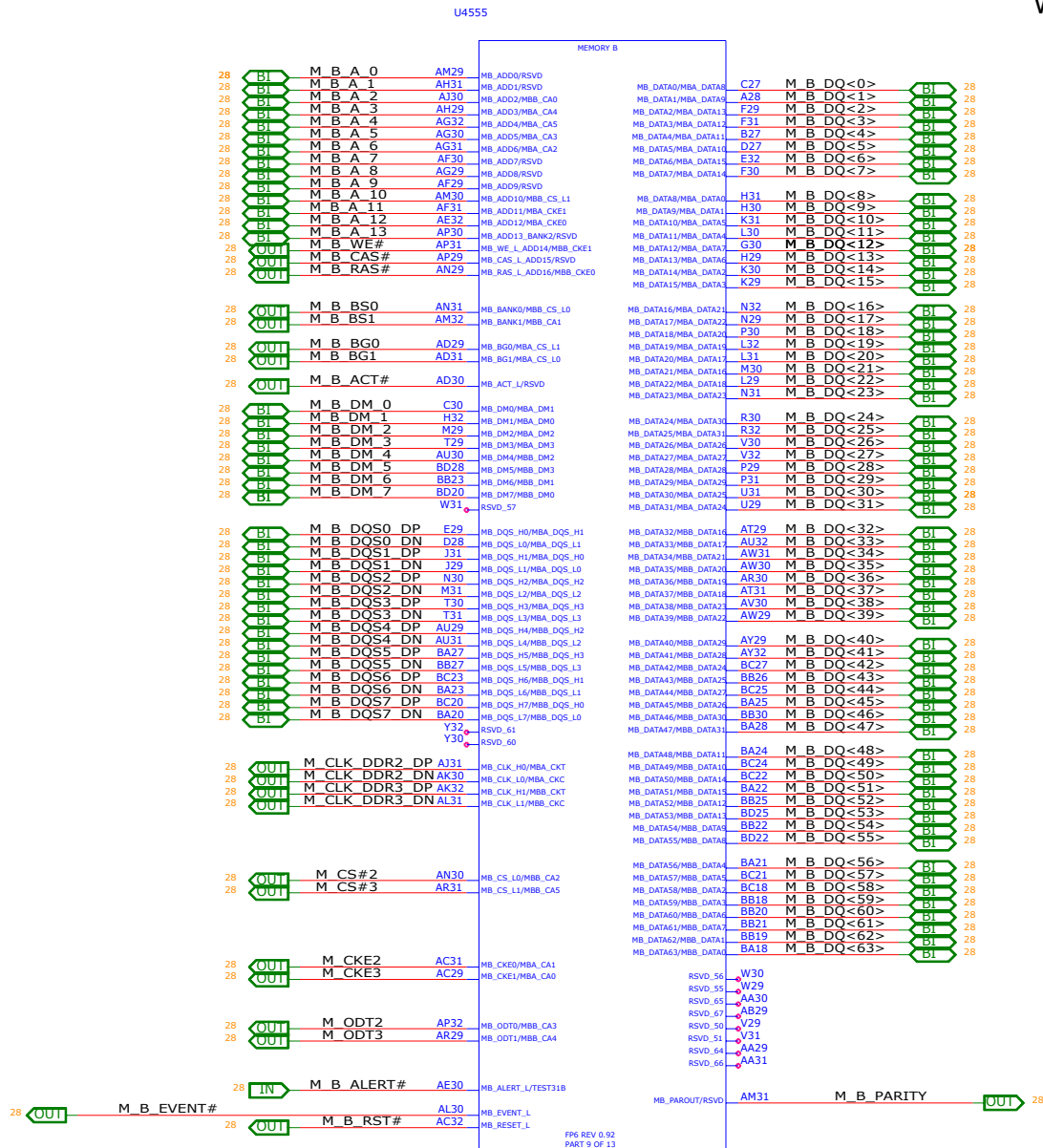
TITLE			
MODEL PROJECT,FUNCTION			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
SHEET 29 of 119			

CHANGE by XXX	DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxx	PCB VER XXX

APU_FP6_MEMORY_CHB

LOCATION NUMBER : 4500~4999(APU)

www.teknisi-indonesia.com



AMD_CEZANNE_H_R7_BGA_FP6_1140P

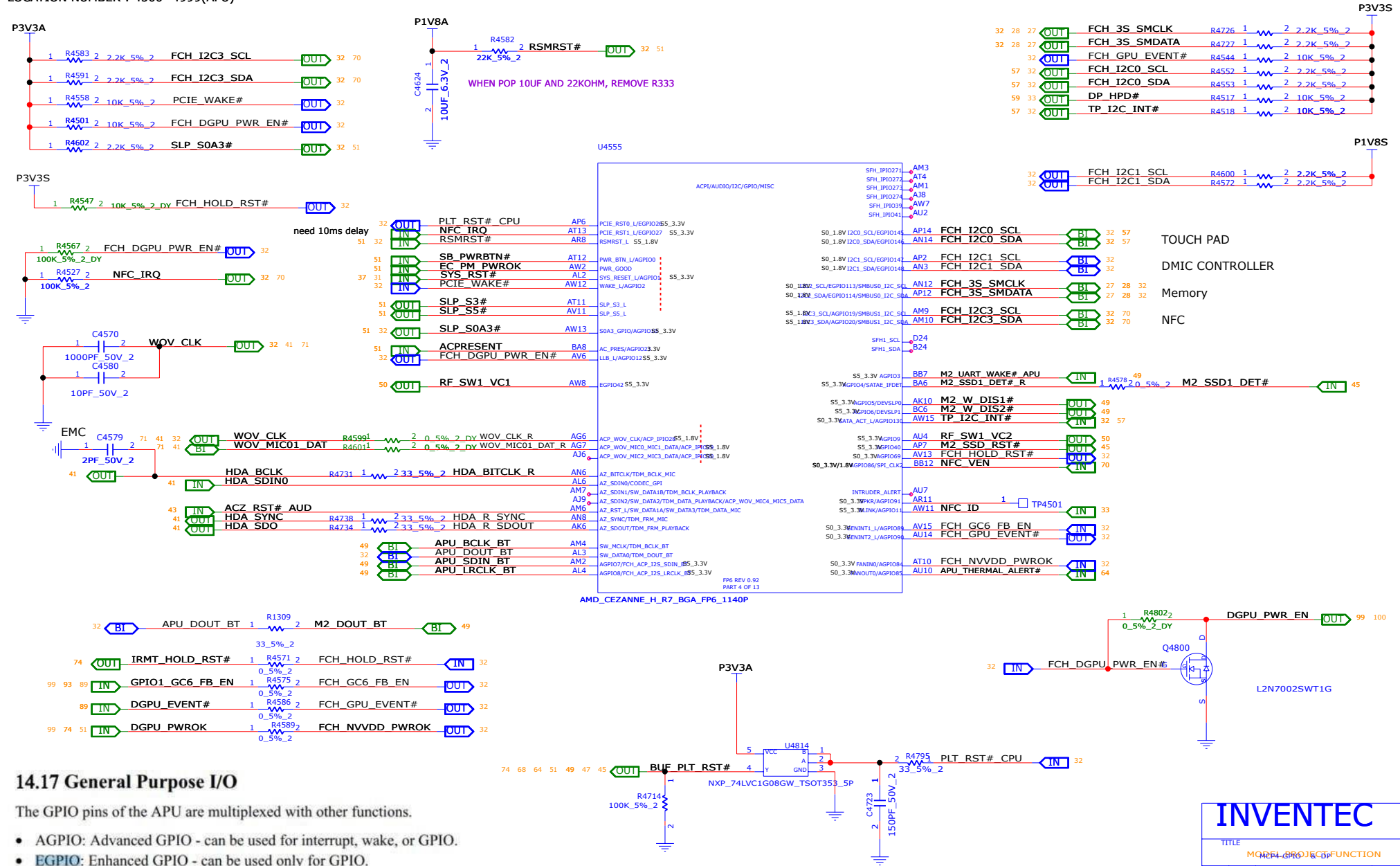
CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	DOC.NUMBER	1310xxxx-0-0	REV	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET	30	of	119				

LOCATION NUMBER : 4500~4999(APU)



APU_FP6_I2C_AUDIO

LOCATION NUMBER : 4500~4999(APU)



14.17 General Purpose I/O

The GPIO pins of the APU are multiplexed with other functions.

- **AGPIO:** Advanced GPIO - can be used for interrupt, wake, or GPIO.
- **EGPIO:** Enhanced GPIO - can be used only for GPIO.

INVENTEC

TITLE		PROJECT		FUNCTION	
M24-00000000		M24-00000000		M24-00000000	
SIZE	A3	DOC NUMBER	1310xxxxx-0-0	REV	X01
SHEET	32	of	119		

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

LOCATION NUMBER : 4500~4999(APU)



TITLE			
MODEL PROJECT,FUNCTION			
MCP5-DDR			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	RE X0
SHEET		33 of 119	

APU_FP6_PCIE/SATA

LOCATION NUMBER : 4500~4999(APU)

U4555

PCIE

GPU

GPU

SSD1

SSD1

LAN

LAN

WLAN

WLAN

SSD2

SSD2

teknisi indonesia

FP6 REV 0.92
PART 2 OF 13

AMD_CEZANNE_H_R7_BGA_FP6_1140P

INVENTEC

TITLE

MODEL & POWER TO FUNCTION

SIZE CODE DOC.NUMBER REV

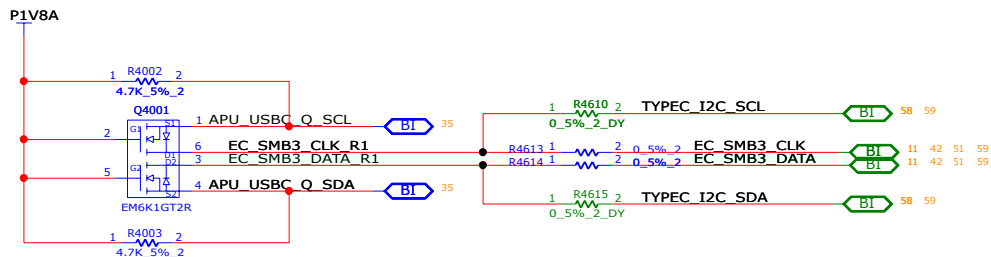
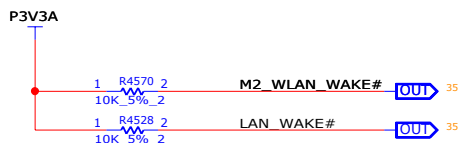
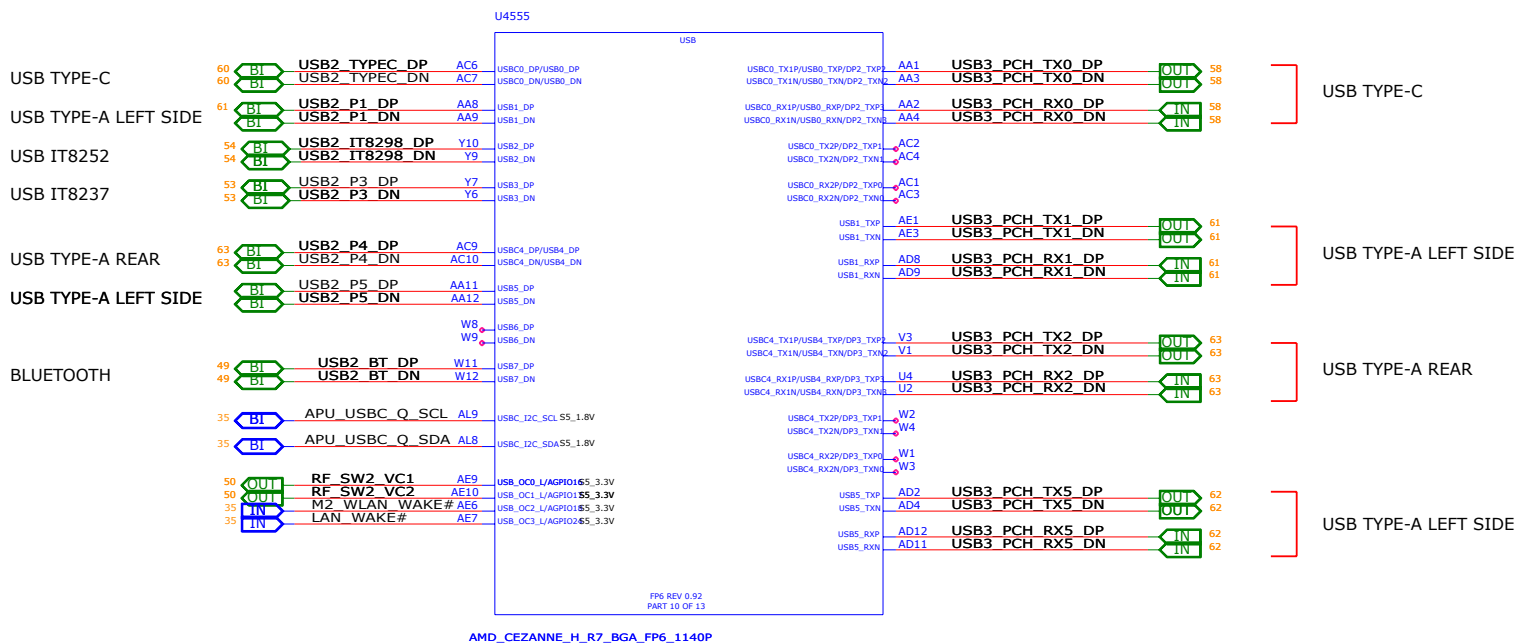
A3 CS 1310xxxx-0-0 X01

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxx PCB VER XXX

SHEET 34 of 119

APU_FP6_USB

LOCATION NUMBER : 4500~4999(APU)



INVENTEC

TITLE

MODEL PROJECT,FUNCTION

SIZE A3

CODE CS

SHEET 35 of 119

DOC.NUMBER 1310xxxx-0-0

REV X01

CHANGE by XXX

PCB P/N 60xxxxxxxxxx

DATE 21-OCT-2002

PCB VER XXX

LOCATION NUMBER : 4500~4999(APU) TWOORE_NB

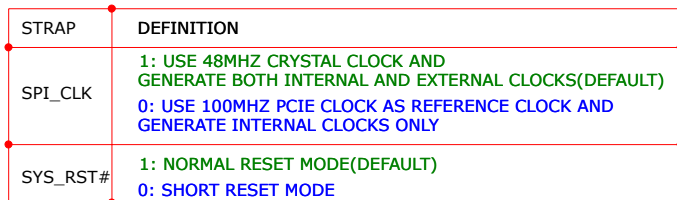
LOCATION NUMBER : 4500~4999(APU)



SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	RE X0
SHEET 36 of 119			

CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	1310xxxxx-0-0	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET	36	of	119		

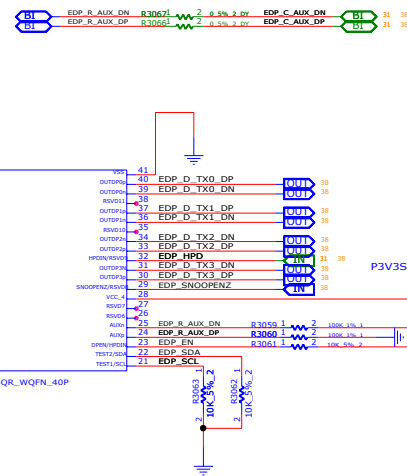
LOCATION NUMBER : 4500~4999(APU)



AGPIO262/WIFIBT_QSPI_DATA2	AGPIO263/WIFIBT_QSPI_DATA3	AGPIO264/WIFIBT_QSPI_CLK		
KB ID0	KB ID1	KB ID2	分配 SKU	註解
0	0	0	1,2,3,5	15" 4 Zone
0	0	1	4	15" PerKey
0	1	0	6,7,8,9,10,11,12	15" PerKey RGB
1	0	0	13,14,15,17	17" 4 Zone
1	0	1	16,18,19	17" PerKey
1	1	0	20,21,22,23,24,25,26	17" PerKey RGB

CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	1310xxxxx-0-0	X01
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX	SHEET 37 of 119			

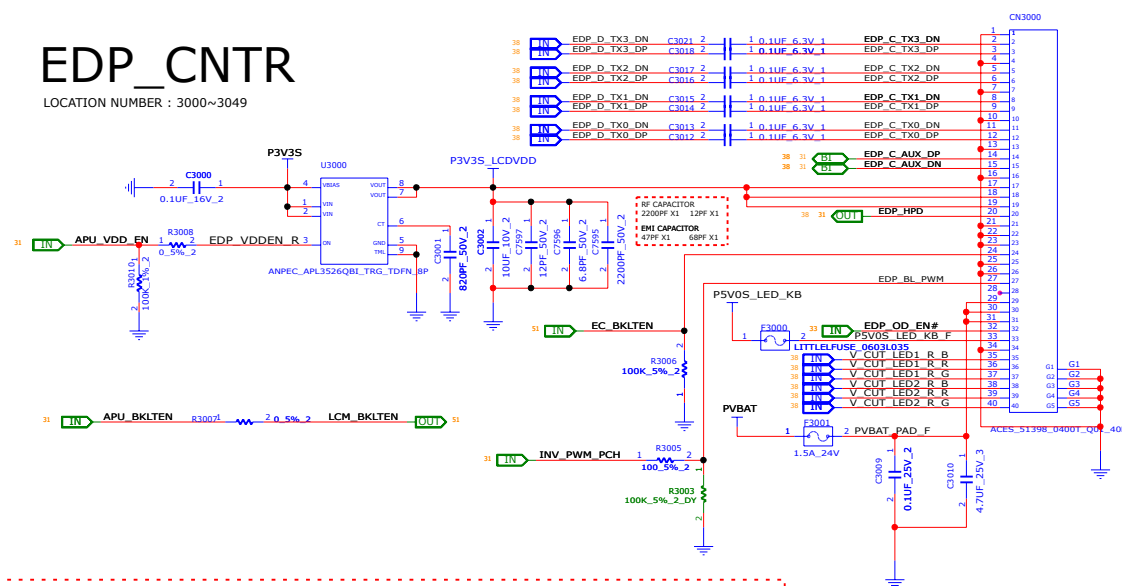
LOCATION NUMBER : 3050~3099



LEVEL	SETTINGS
0	Option 1: Tie 1 kΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 kΩ 5% to GND.
F	Float (leave pin open)
1	Option 1: Tie 1 kΩ 5% to V_{CC} . Option 2: Tie directly to V_{CC} .

EDP CNTR

LOCATION NUMBER : 3000~3049

[illegible]

SCAR : R3545 DY

INVENTEC

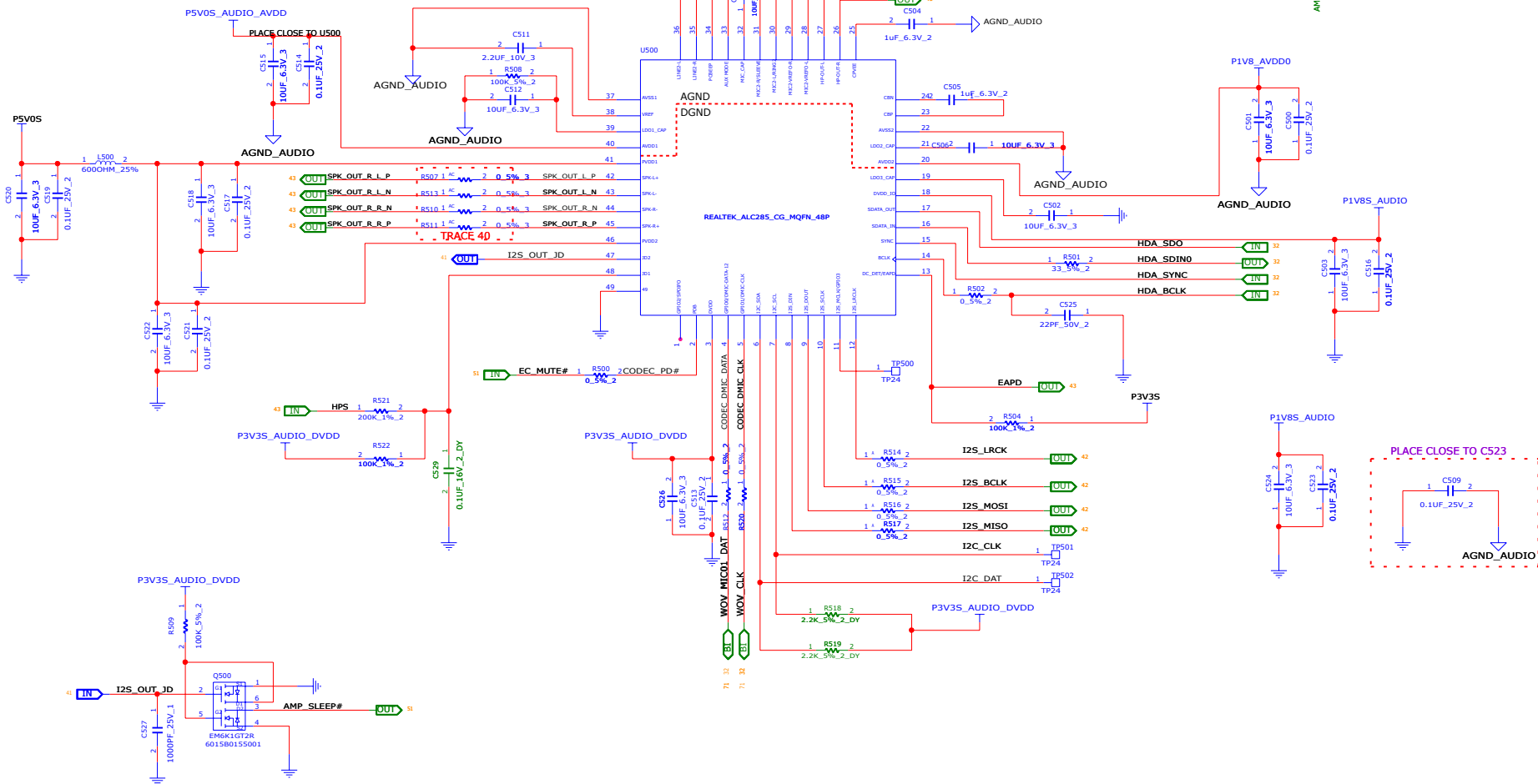
TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC. NUMBER 1310xxxxxx-0-0	X
SHEET 38 of 119			

CHANGE BY	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	DOC NUMBER	1310XXXXX-0-0	
PCB P/N	60XXXXXXXXXX	PCB VER	XXX			SHEET	38	of	119	

LOCATION NUMBER : 3200~3299



LOCATION NUMBER : 500~549



INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310XXXXXX-0-0	REV X01
SHEET		41	of 119

CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	DOC NUMBER	1310XXXXXX-0-0	REV	X01
PCB P/N	60XXXXXXXXXX	PCB VER	XXX			SHEET	41	of	119		

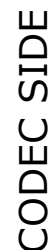
LOCATION NUMBER : 550~599



TITLE				R X
MODEL,PROJECT,FUNCTION Block Diagram				
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0		
SHEET		42 of 119		

CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	1310xxxxx-0-0	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET		42	of	119	
3		2			1				

LOCATION NUMBER : 600~699(SPK)
LOCATION NUMBER : 9000~9099(JACK)



The diagram illustrates a 40-pin connector interface with two main sections: RF (Radio Frequency) and EMI (Electromagnetic Interference).

RF Section: This section is enclosed in a red dashed box at the top right. It contains four parallel LC matching networks, each consisting of a series capacitor (C618, C610, C611, C617) and a shunt inductor (L600, L601, L602, L603). The capacitors are labeled 12PF 50V 2 DY. The inductors are labeled AC L600, AC L601, AC L602, and AC L603. The RF signals are connected to pins 1, 2, 3, and 4 of the connector.

EMI Section: This section is enclosed in a red dashed box at the bottom. It contains four parallel LC matching networks, each consisting of a series capacitor (C608, C609, C607, C606) and a shunt inductor (L604, L605, L606, L607). The capacitors are labeled 1000PF 50V 2. The inductors are labeled AC L604, AC L605, AC L606, and AC L607. The EMI signals are connected to pins 5, 6, 7, and 8 of the connector.

Connector and Grounding: The connector is a 40-pin D-sub connector. The ground pins (pins 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40) are connected to a common ground plane. The ground plane is labeled GND and is connected to the chassis ground.

Component Values: The component values are as follows:

- Capacitors: C618, C610, C611, C617 (12PF 50V 2 DY); C608, C609, C607, C606 (1000PF 50V 2).
- Inductors: L600, L601, L602, L603 (AC); L604, L605, L606, L607 (AC).

Placement: The EMI components are labeled "EMI" and "PLACEMENT NEAR CONNECTOR".

INVENTEC

				TITLE MODEL, PROJECT, FUNCTION Block Diagram			
CHANGE #	XXX	DATE	21-OCT-2002	SIZE	CODE	DOC. NUMBER	REV
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX	A3	CS	1310xxxxxx-0-0	X01
				SHEET 43 of 119			

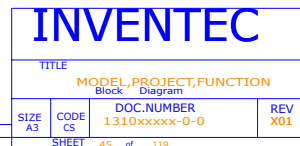
8	7	6	5	4	3	2	1
D							
C							
B							
A							
8	7	6	5	4	3	2	1

RESERVE

INVENTEC

CHANGE by	XXX	DATE	21-OCT-2002	SIZE	CODE	DOC. NUMBER	REV
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	A3	CS	1310xxxx-0-0	X01
				SHEET	44 of 119		

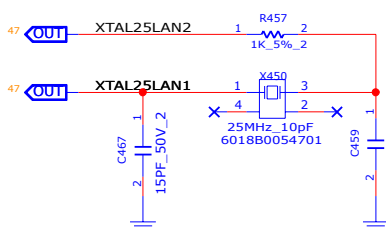
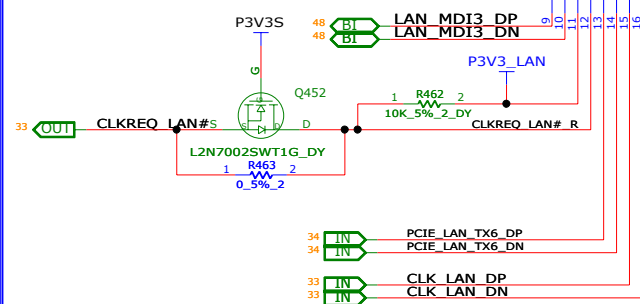
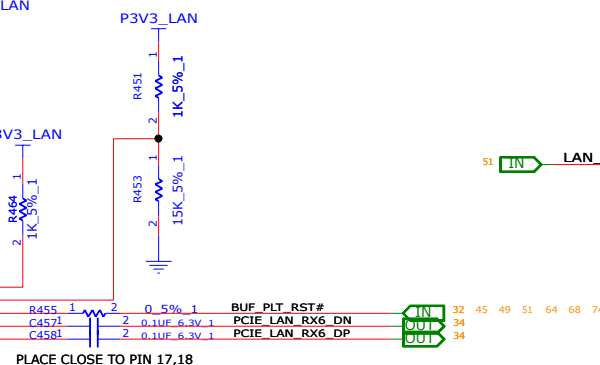
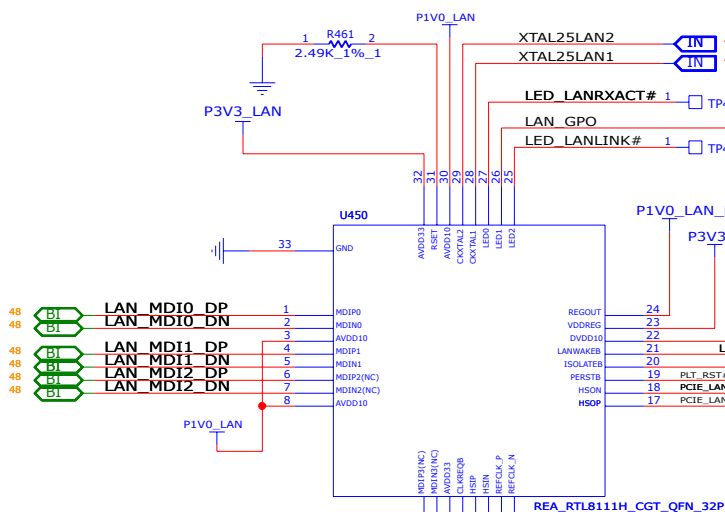
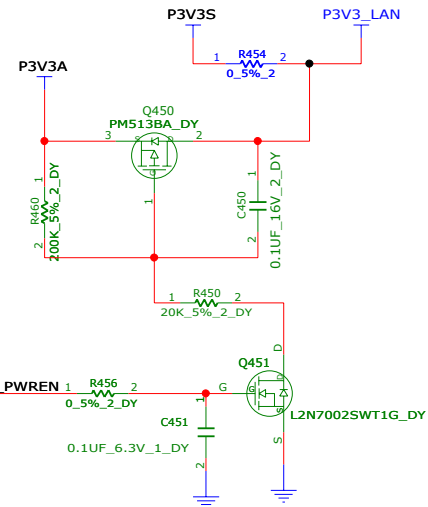
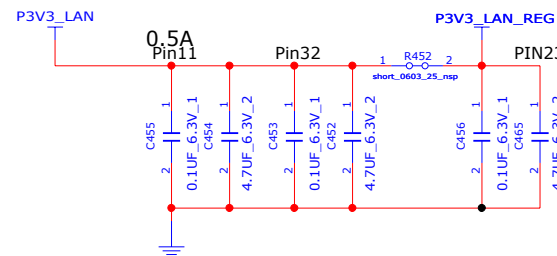
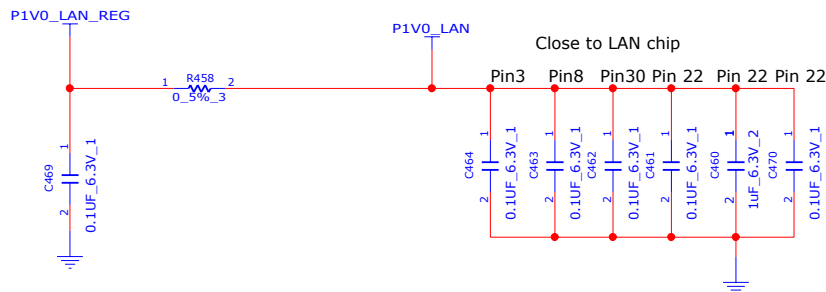
LOCATION NUMBER : 1900~1949



LAN (RTL8111H)

LOCATION NUMBER : 450 ~ 479

P3V3_LAN RISING TIME (10%~90%)要>0.5MS AND <100MS
LAN POWER NOISE P3V3_LAN < 200MV VPEAK TO VPEAK.
LAN POWER NOISE P1V0_LAN < 100MV VPEAK TO VPEAK.



INVENTEC

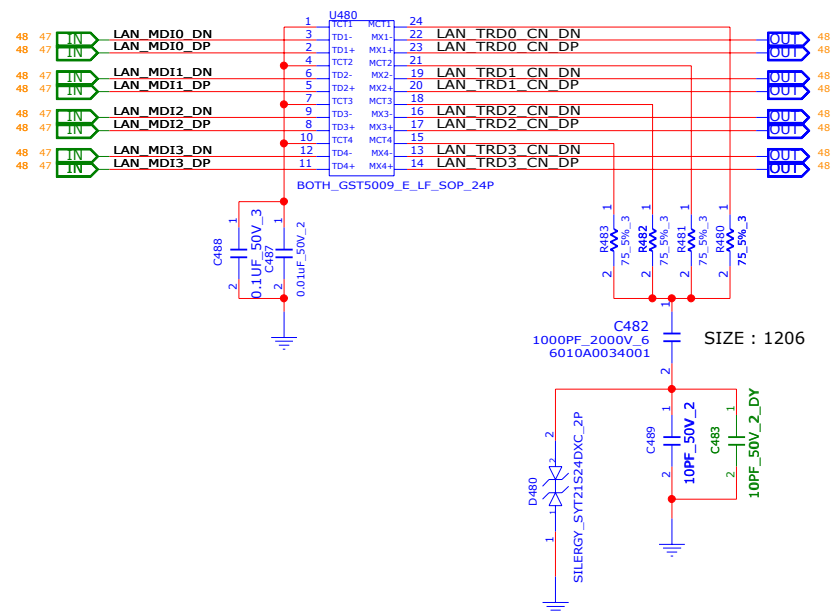
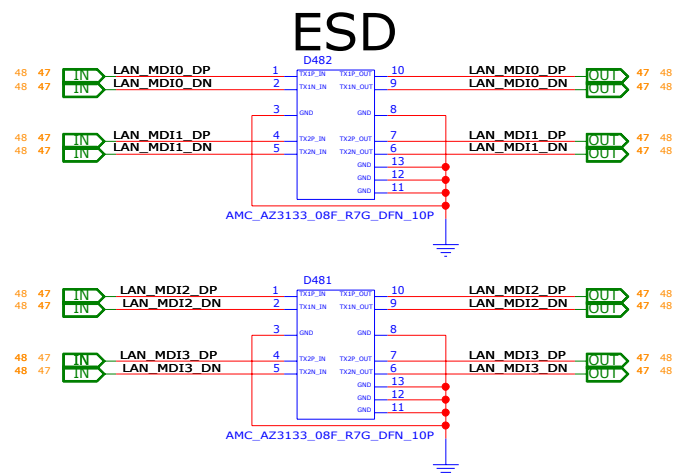
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
DOC. NUMBER			
1310xxxx-0-0			
REV			
X01			

CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	SHEET	47 of 119
PCB P/N	60xxxxxxxxxx	PCB VER	XXX						

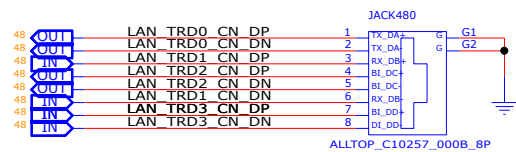
LAN (RTL8111H)

LOCATION NUMBER : 480 ~ 499

TRANSFORMER



RJ-45



INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

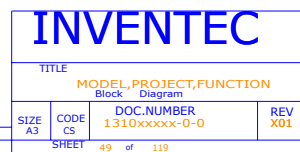
SIZE A3 CODE CS
SHEET 48 of 119

REV X01

CHANGE by XXX
PCB P/N 60xxxxxxxxxx

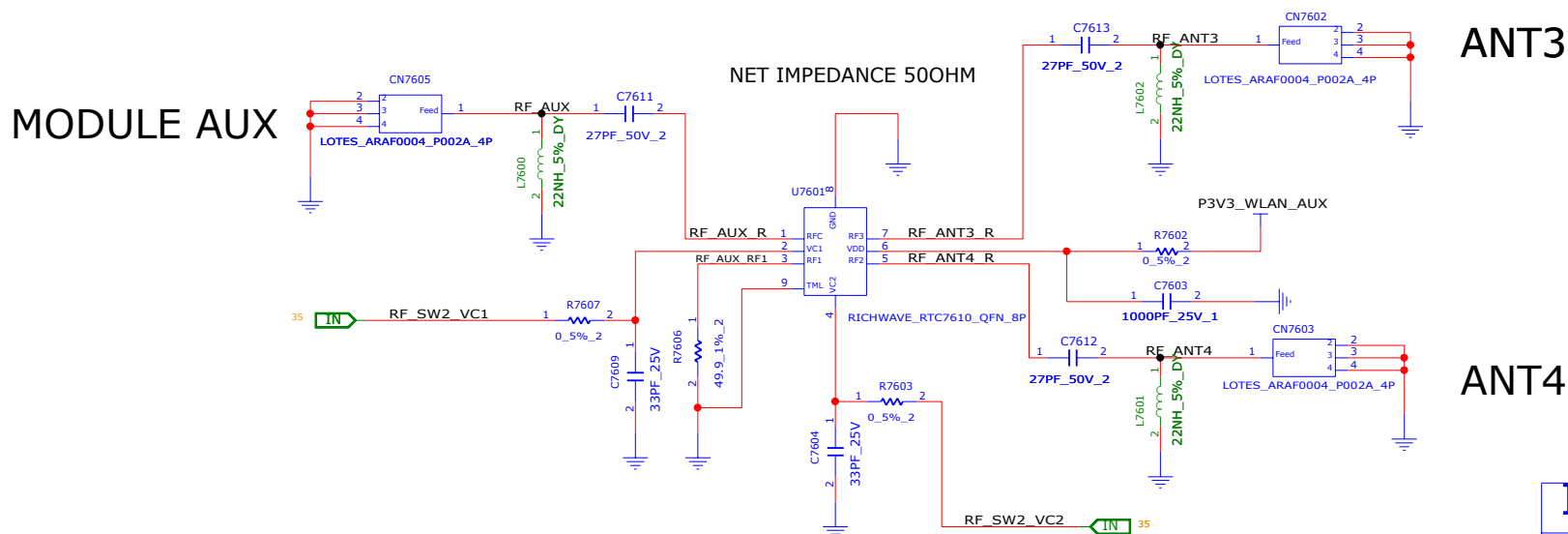
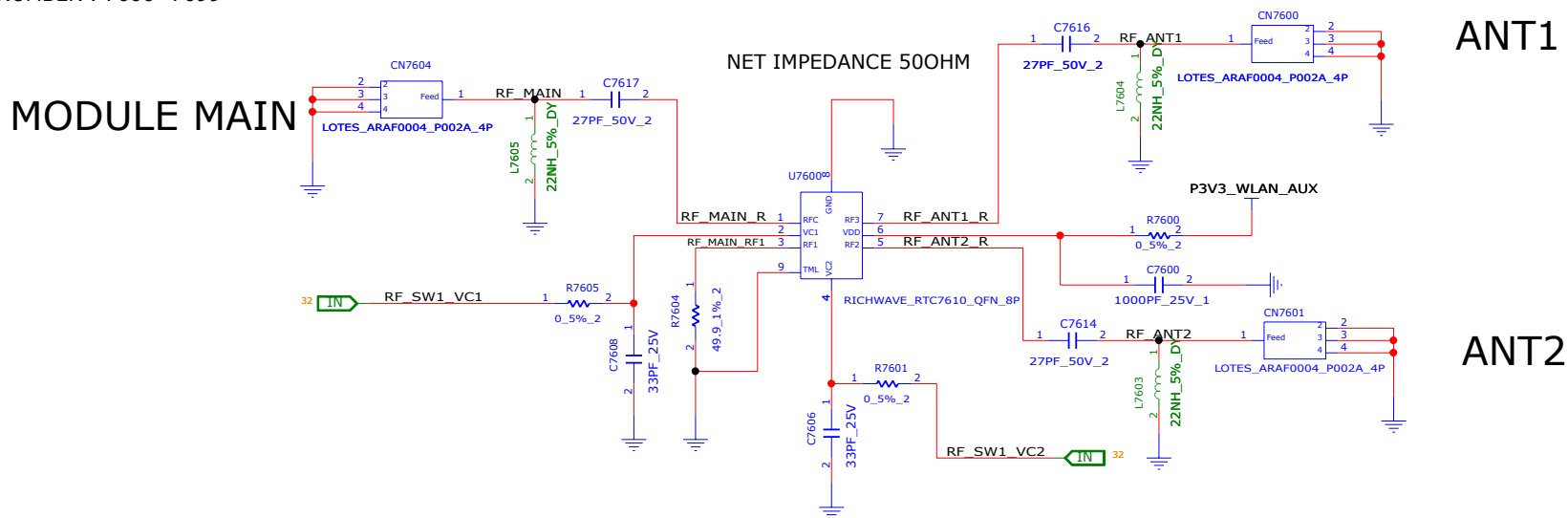
DATE 21-OCT-2002
PCB VER XXX

LOCATION NUMBER : 1300~1399



RF CONN

LOCATION NUMBER : 7600~7699



INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block		Diagram	
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		50 of 119	

CHANGE by	xxx
PCB P/N	60xxxxxxxxxxx

DATE	21-OCT-2002
PCB VER	XXX

SIZE A3	CODE CS	1310xxxxx-0-0	X01
SHEET		50 of 119	

LOCATION NUMBER : 300~399

[illegible]

LOCATION NUMBER : 8000~8199



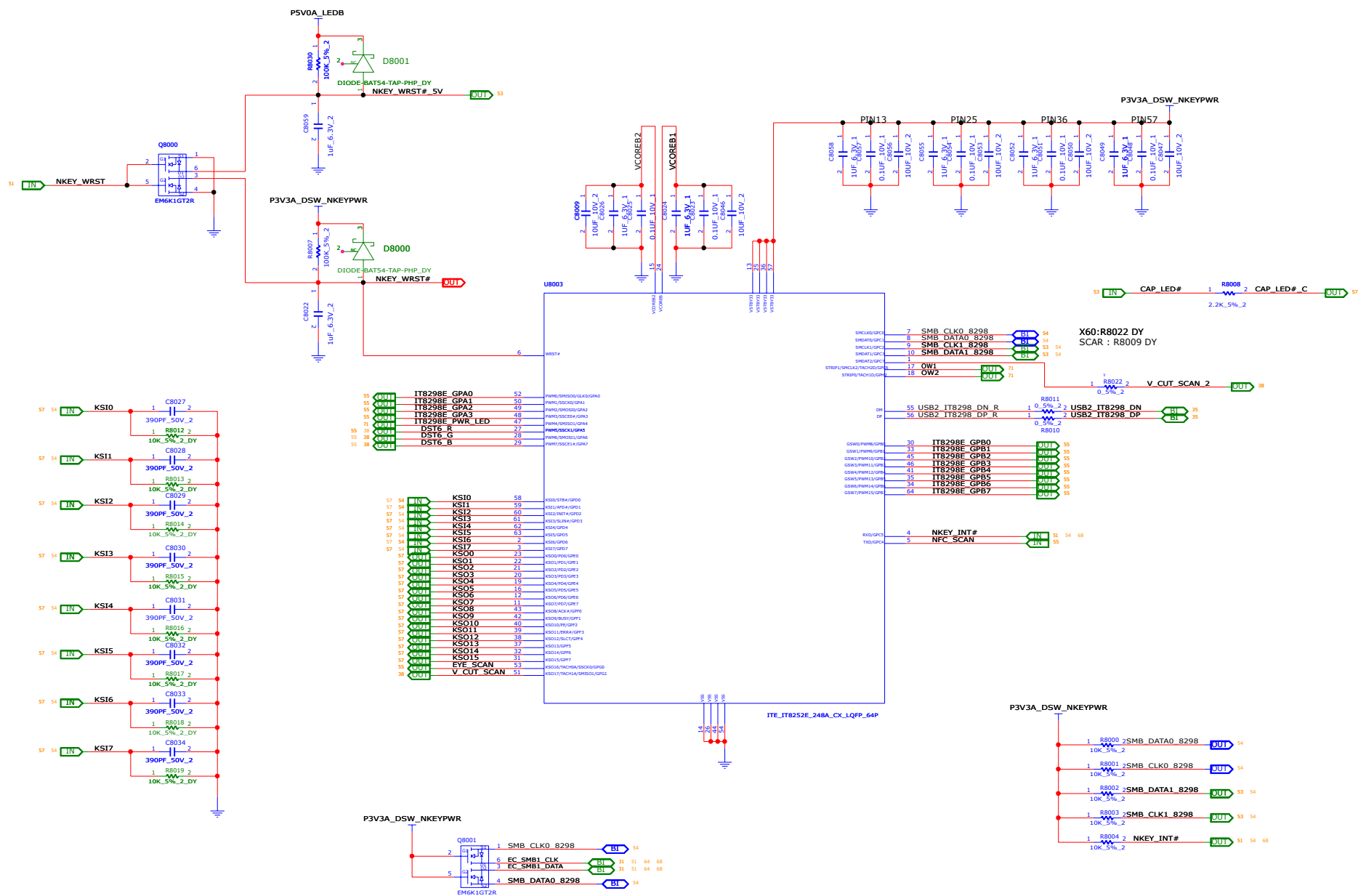
teknisi indonesia

INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
		Block	Diagram
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxxx-0-0	REV X01
SHEET		53	of 119

IT8252E

LOCATION NUMBER : 8000~8199



INVENTEC

TITLE		MODEL/PROJECT/FUNCTION		DOC NUMBER		REV	
Block		Diagram		1310xxxx-0-0		X01	
SIZE	A7	CODE	CS	SHEET	54	of	110

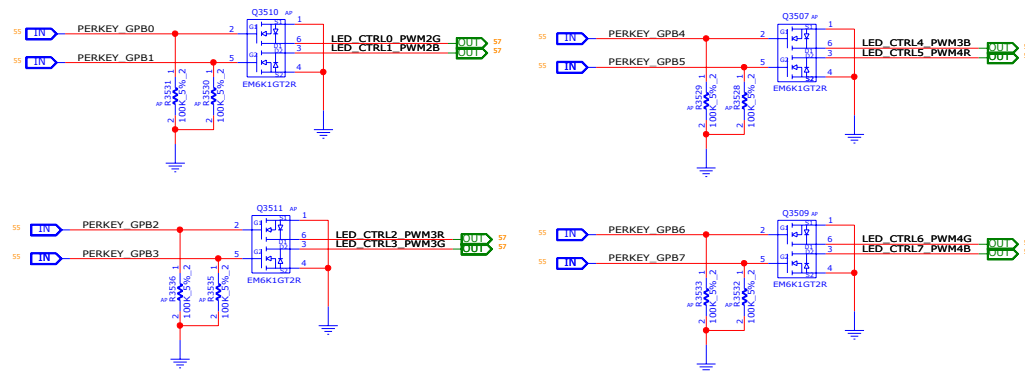
CHANGE BY	XXX	DATE	21-OCT-2002
PCB P/N	8199xxxxxx	PCB VER	XXX

KB/EAGLE EYE RGB LED

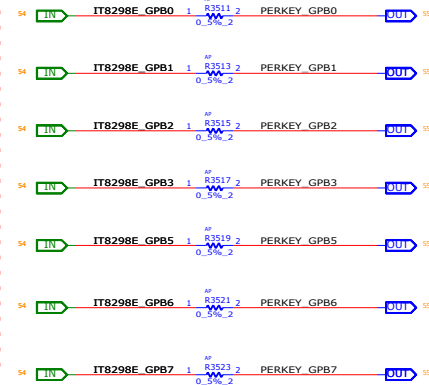
LOCATION NUMBER : 3500~3599

KB RGB PER KEY LED

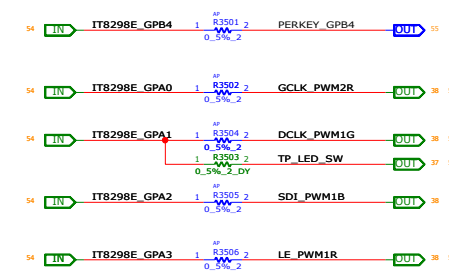
MAX:960MA



SCAN LINE

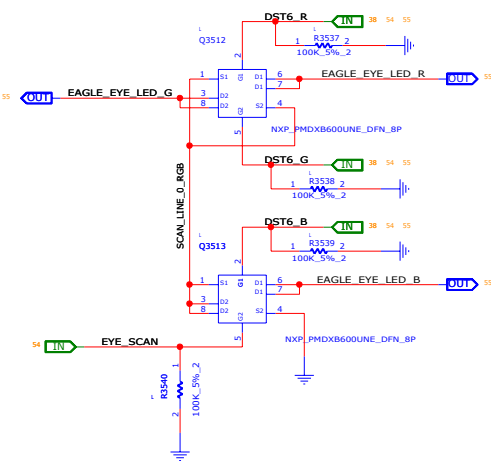


LAUNCH KEY

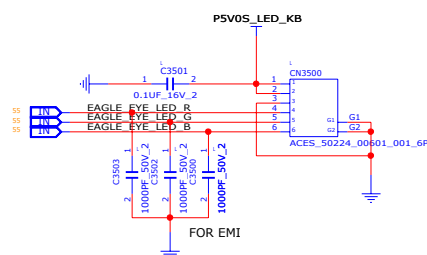


EAGLE EYE LED

MAX:525MA



EAGLE EYE LED CONN

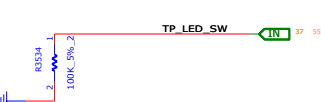


KB RGB 4ZONE LED

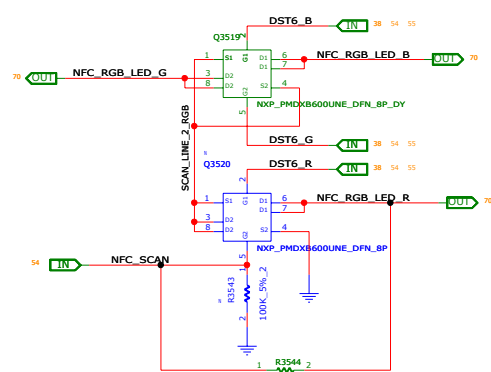
MAX:494.5MA



TP LED



NFC RGB LED



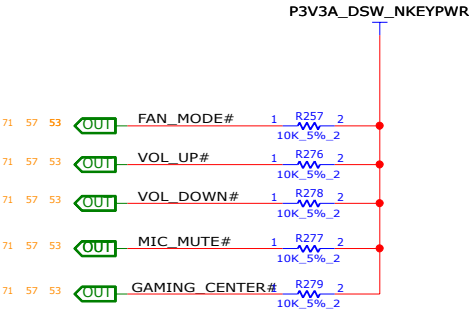
INVENTEC

CHANGE BY		DATE	21-OCT-2002	SIZE	A7	CODE	CS	DOC NUMBER	1310xxxx-0-0	REV	X01
PCB P/N		PCB VER	XXX	SHEET		55	of	110			

IT8013

LOCATION NUMBER : 250~279

IT8013	LED_TYPE SELECT 3V3	KB Type
GP5	H	PerKey
GP5	L	4 Zone/1 Zone RGB



INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

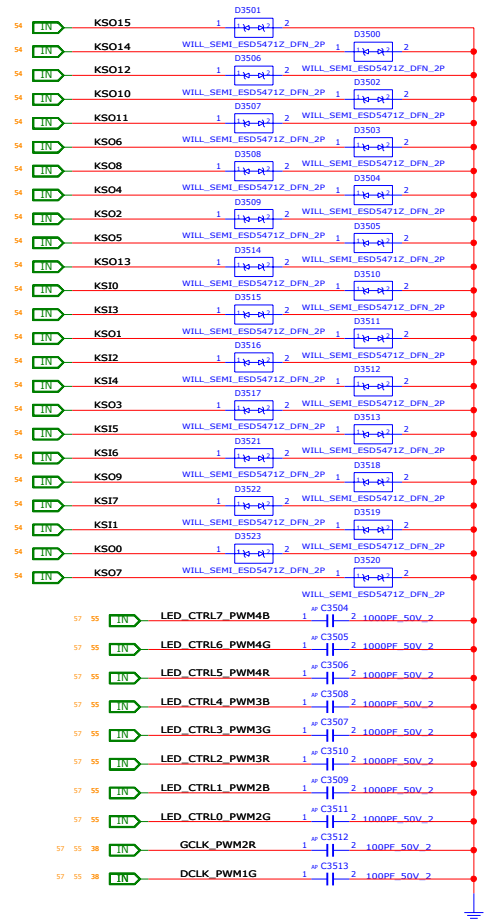
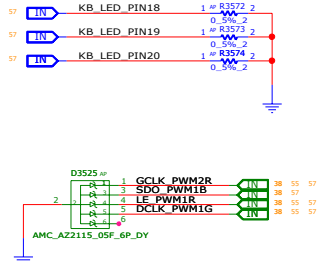
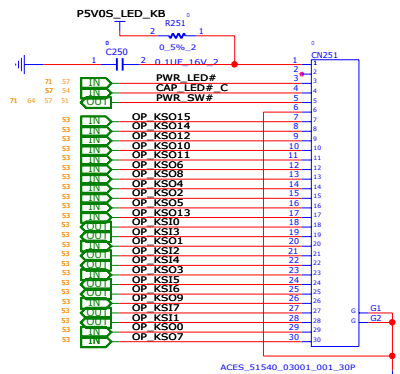
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET	56	of 119	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

KB CNTR/TOUCH PAD

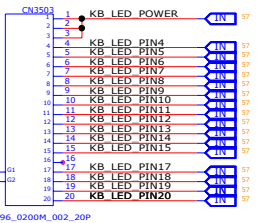
LOCATION NUMBER : 250~279(KEYBOARD)
LOCATION NUMBER : 280~299(TP CNTR)

KEYBOARD CONN

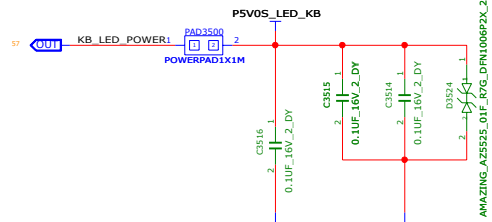


KEYBOARD BACKLIGHT

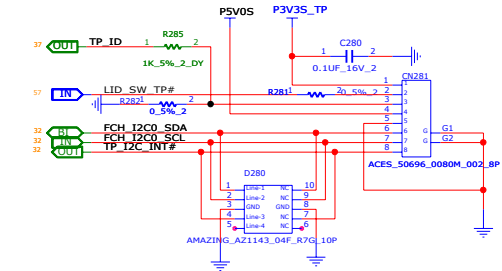
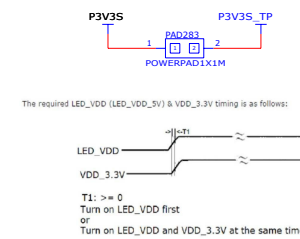
PERKEY



4ZONE



TOUCHPAD

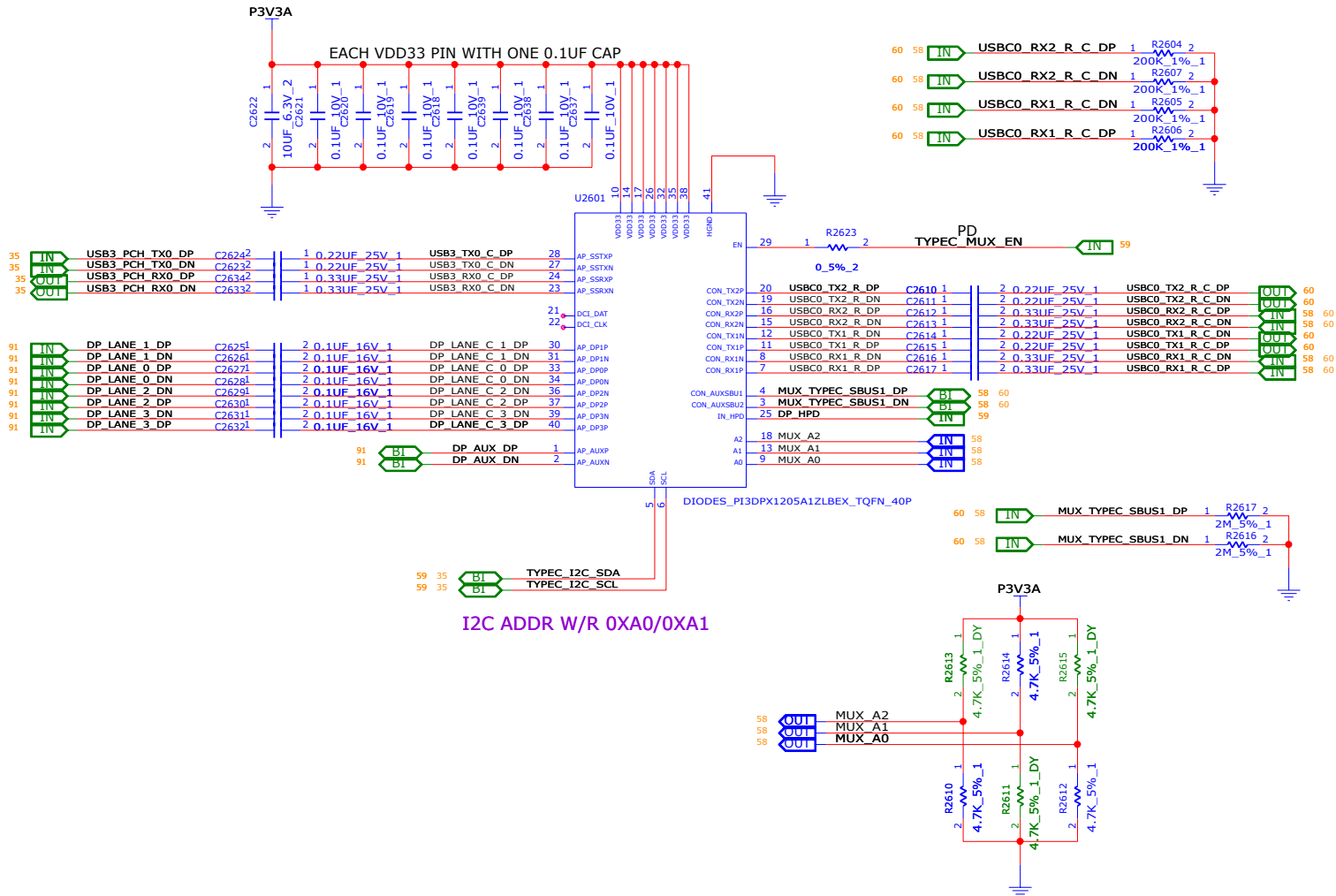


INVENTEC

CHANGE	BY	DATE	21-OCT-2002
PCB P/N	XXXXXXXXXXXX	PCB VER	XXX
SIZE	A1	CODE	13100CXXXX-C-0
SHEET	57	REV	001

TYPEC REDRIVER

LOCATION NUMBER : 2600~2699



INVENTEC

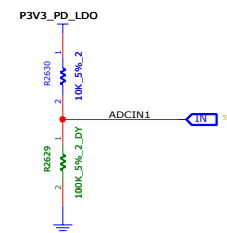
TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET		58 of 119	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

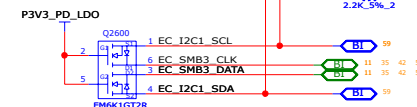
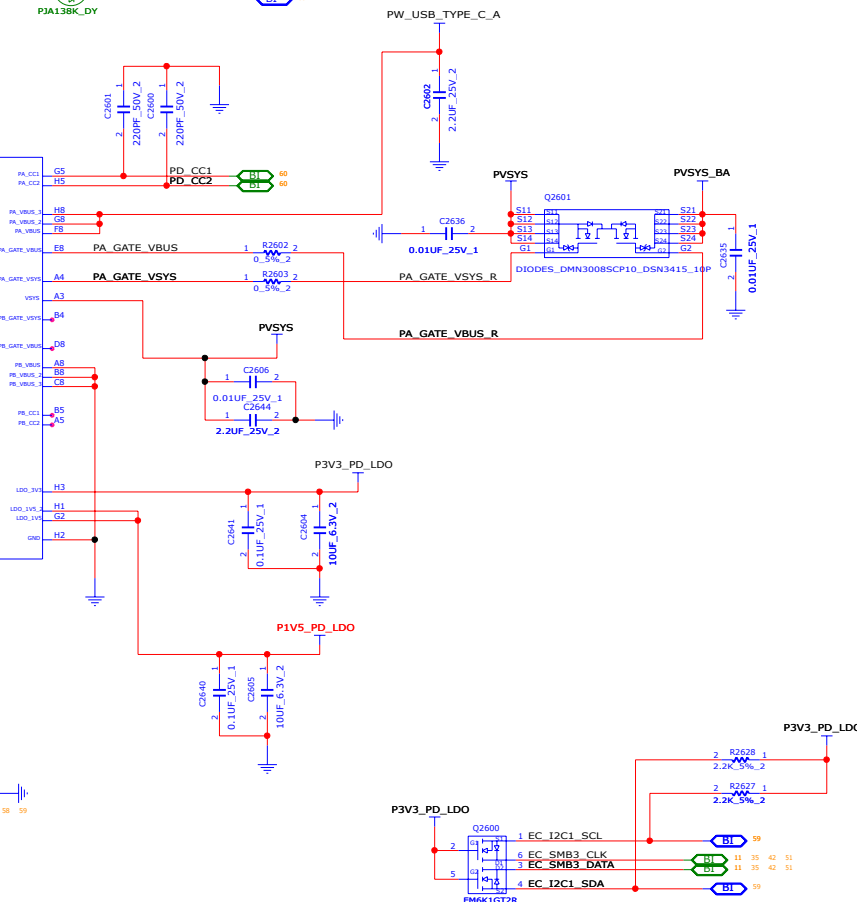
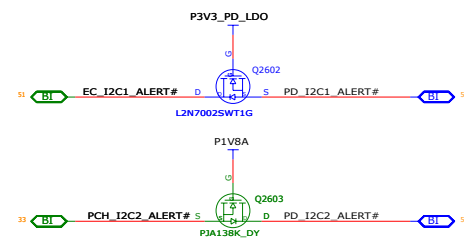
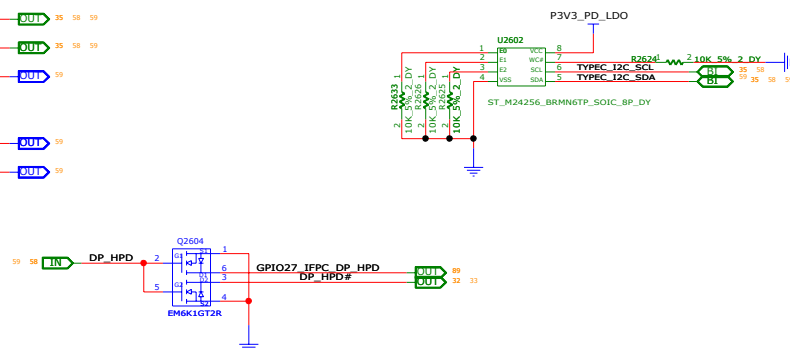
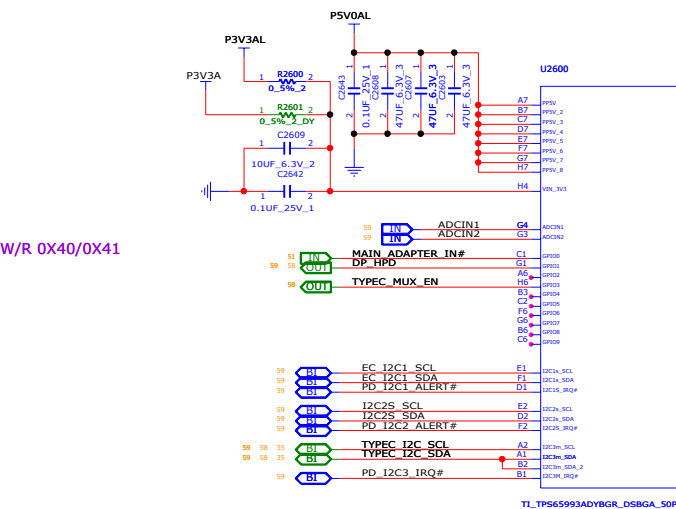
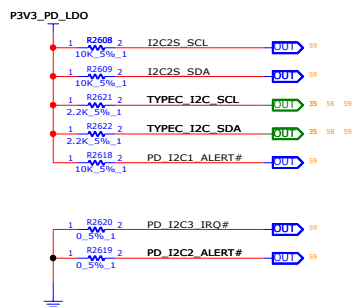
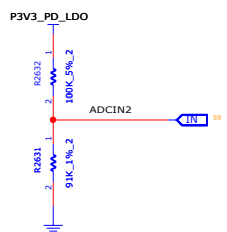
LOCATION NUMBER : 2600~2699

DIV = RDOWN / (RUP + RDOWN) ⁽¹⁾			Without using RUP or RDOWN	ADCINx decoded value
MIN	Target	MAX		
0	0.0114	0.0228	tie to GND	0
0.0229	0.0475	0.0722	N/A	1
0.0723	0.1074	0.1425	N/A	2
0.1425	0.1899	0.2372	N/A	3
0.2373	0.3022	0.3671	N/A	4
0.3672	0.5368	0.7064	tie to LDO_1V5	5
0.7065	0.8062	0.9060	N/A	6
0.9061	0.9530	1.0	tie to LDO 3V3	7

(1) External resistor tolerance of 1% is recommended. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values. For convenience, the Target column shows this value.

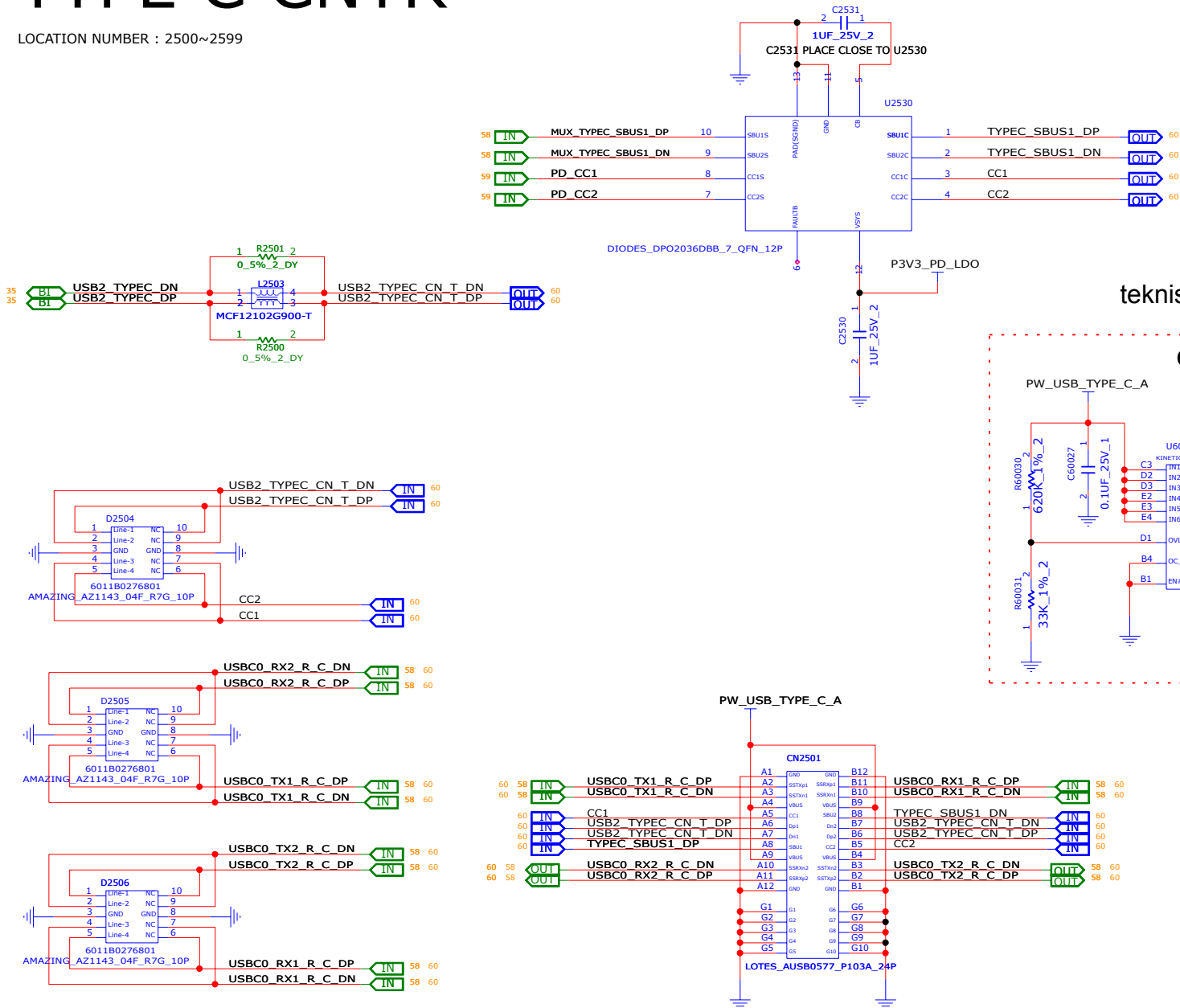


I2C ADDR W/R 0X40/0X41



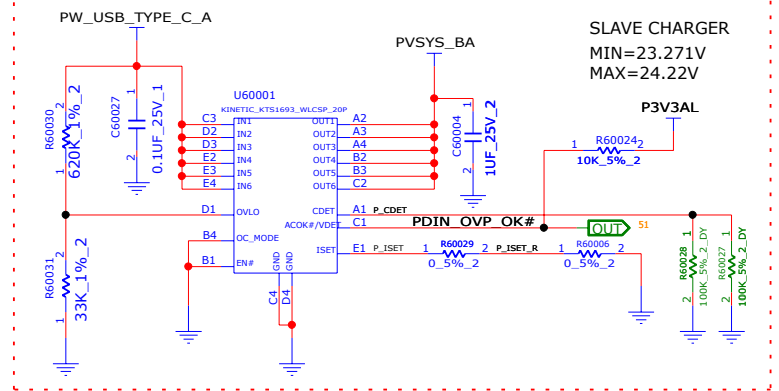
TYPE C CNTR

LOCATION NUMBER : 2500~2599



teknisi indonesia

OVP FOR TYPEC INPUT



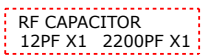
SLAVE CHARGER
MIN=23.271V
MAX=24.22V

INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET	60 of 119		

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

LOCATION NUMBER : 2450~2499

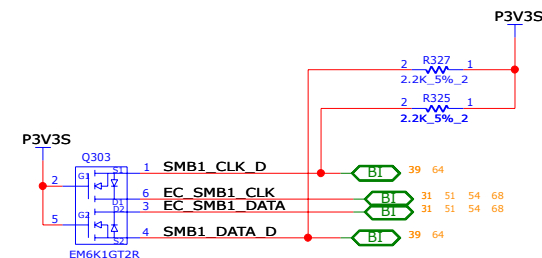
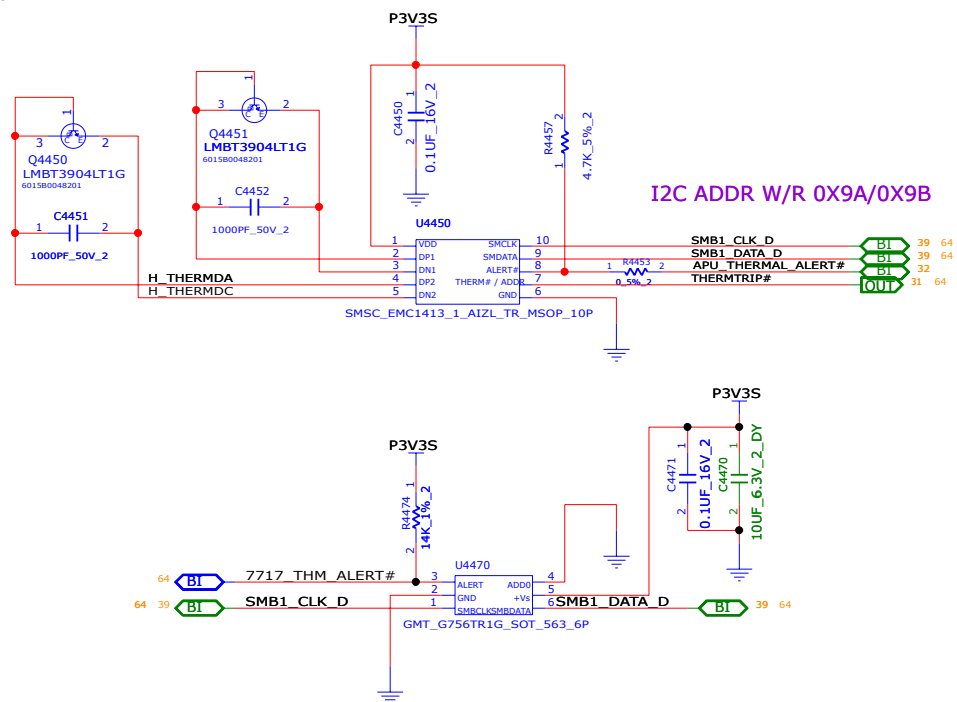


TITLE	MODEL, PROJECT, FUNCTION
	Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	1310xxxxx-0-0	X01
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX	SHEET 62 of 119			
3		2		1			

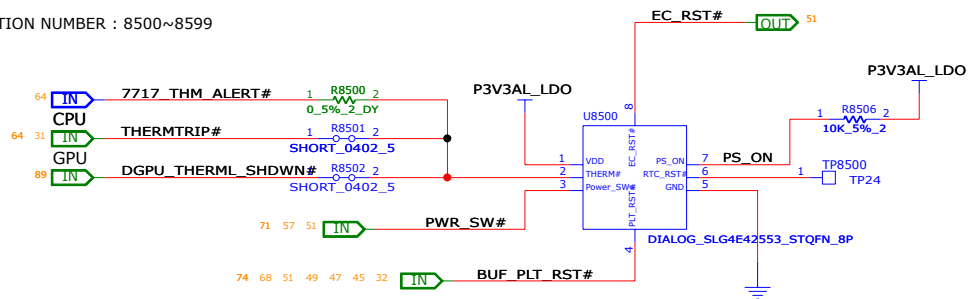
THERM SENSOR

LOCATION NUMBER:4450~4499



EC_SHUTDOWN

LOCATION NUMBER : 8500~8599



INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		64 of 119	

CHANGE by		XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	1310xxxxx-0-0	X01
PCB P/N		60xxxxxxxxxxx	PCB VER	XXX	SHEET		64 of 119			
3			2			1				

LOCATION NUMBER : 4400~4449



TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		65 of 119	

CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	1310xxxxx-0-0	X01
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX	SHEET 65 of 119			

LOCATION NUMBER : 7 500~75 99



CHANGE BY	8-89	DATE	21-JUNE-2002								
<table border="1"> <tr> <td>SIZE</td> <td>CODE</td> <td>DOC NUMBER</td> <td>REV</td> </tr> <tr> <td>A3</td> <td>CS</td> <td>13.10.000000.0-0</td> <td>A01</td> </tr> </table>				SIZE	CODE	DOC NUMBER	REV	A3	CS	13.10.000000.0-0	A01
SIZE	CODE	DOC NUMBER	REV								
A3	CS	13.10.000000.0-0	A01								
TITLE											
MODEL PROJECT FUNCTION											

1

1

1

4

1

1

1

4

1

1

1

4

1

1

1

4

1

1

1

10

7

1

1

1

1

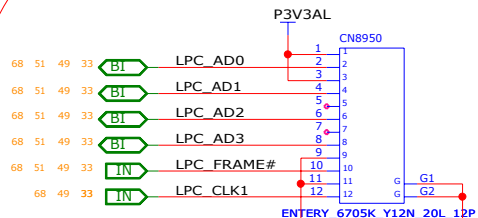
1

10

DEBUG CONN

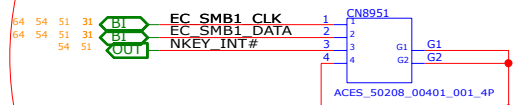
LOCATION NUMBER : 8950~8999

ASUS LPC DEBUG

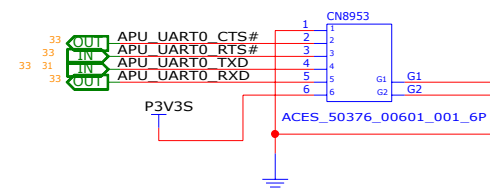


CHANGE TO ASUS CN

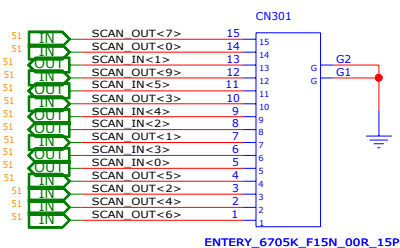
N-KEY DEBUG



CHANGE TO ASUS CN

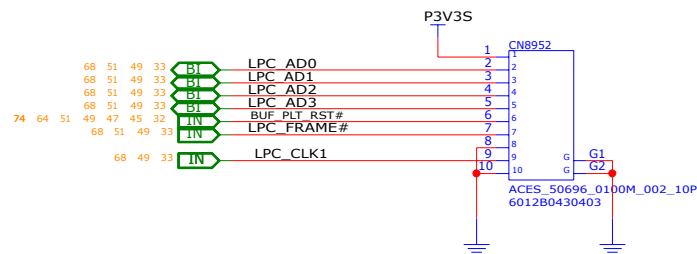


FOR ROM FLASH



CHANGE TO ASUS CN

IEC LPC DEBUG



INVENTEC

TITLE	MODEL, PROJECT, FUNCTION
Block	Diagram

SIZE	CODE	DOC.NUMBER
12	22	1310xxxxxx-0-0

REV
X01

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60XXXXXXXXXX	PCB VER	XXX

A3 CS SHEET 68 of 119

68 of 119

	8	7	6	5	4	3	2	1
D								
C								
B								
A								
	8	7	6	5	4	3	2	1

RESERVED

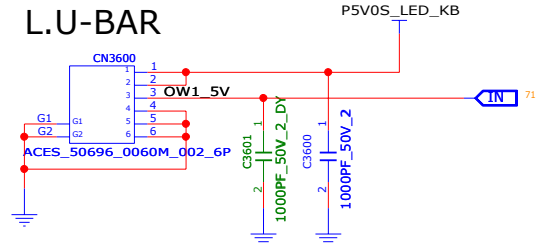
INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block / Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 69 of 119			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

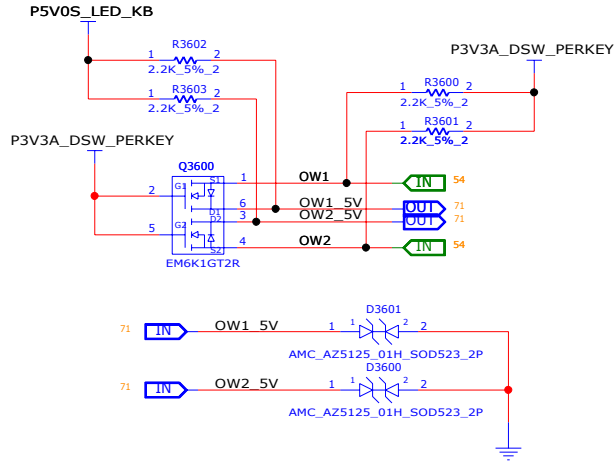
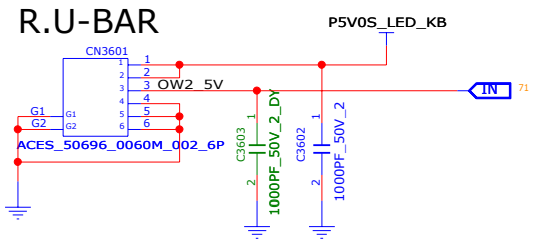
MB_L.U/R.U-BAR/INDICATOR/MIC

LOCATION NUMBER : 3500~3699

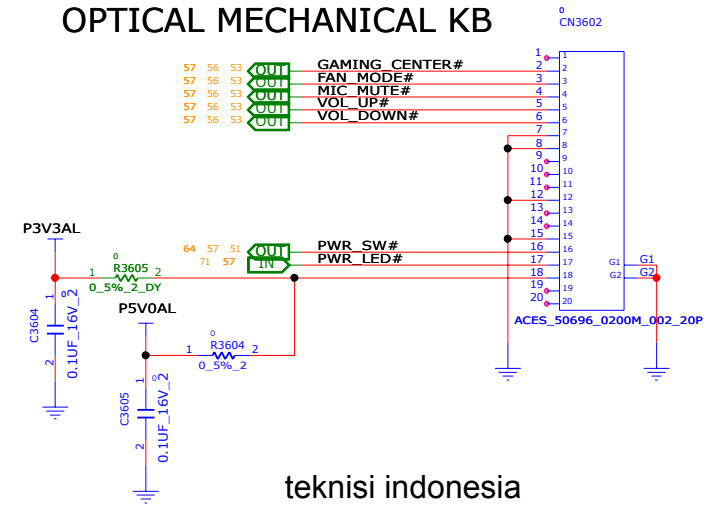
L.U-BAR



R.U-BAR

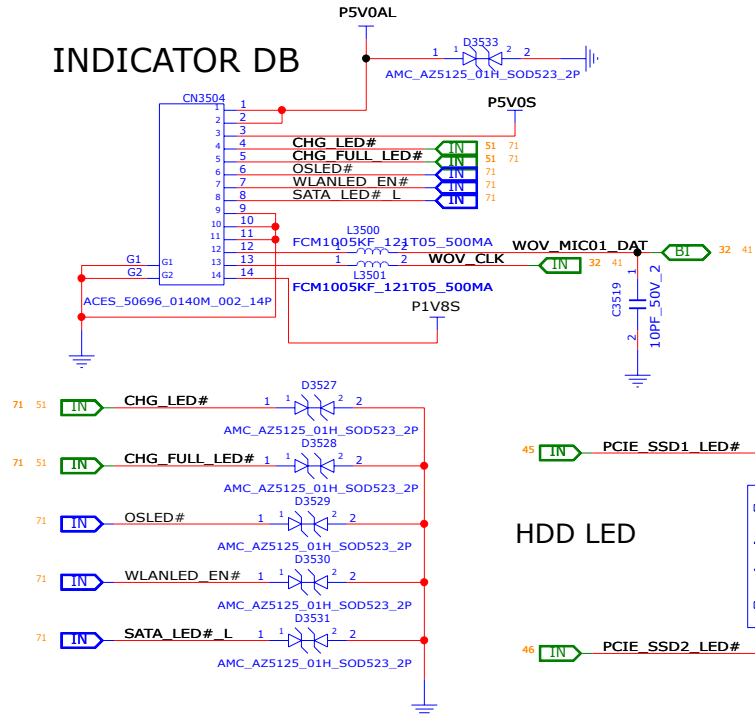


OPTICAL MECHANICAL KB

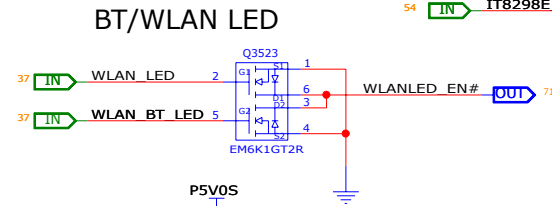


teknisi indonesia

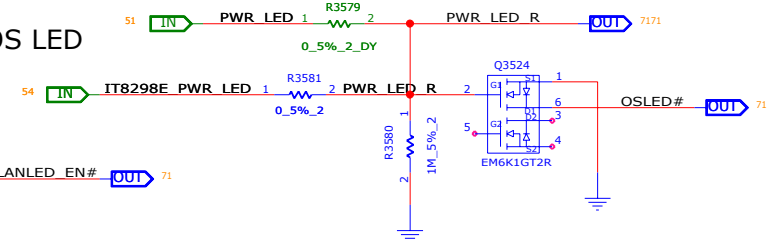
INDICATOR DB



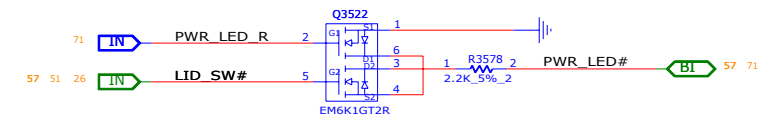
BT/WLAN LED



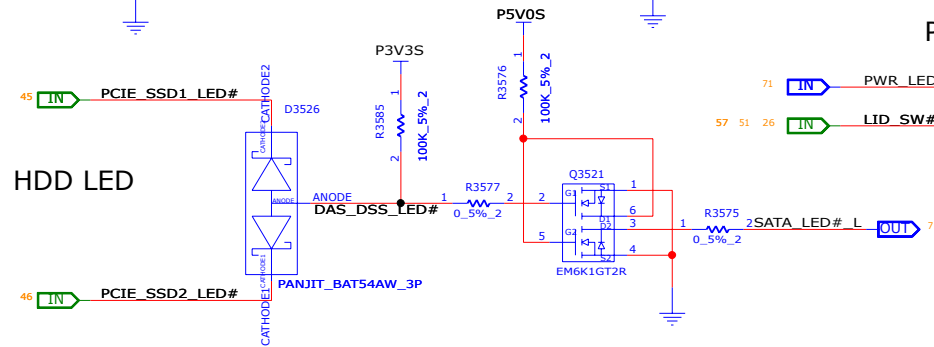
OS LED



POWER KEY LED



HDD LED



INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET	71	of 119	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

8	7	6	5	4	3	2	1
D							
C							
B							
A							
8	7	6	5	4	3	2	1

GN20 E7

8GB GDDR6 256M X 16 X 2 X6

INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block / Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 72 of 119			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

07e409180c100f00520f7a8d74001513

CHANGE by	XXX	DATE	21-OCT-2002	A3	CS	1510XXXX-0-0	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET 73 of 119			

LOCATION NUMBER : 5000~5499



SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0	REV X01
SHEET		74	of 119

CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	DOC NUMBER	1310XXXXX-0-0	REV	X01
PCB P/N	60XXXXXXXXXX	PCB VER	XXX	SHEET		74	of		119		

LOCATION NUMBER : 5000~5499

[illegible]

112

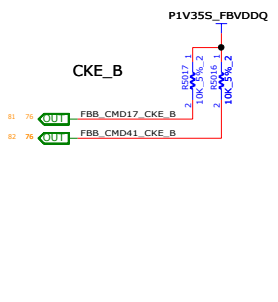
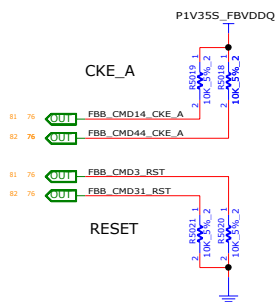
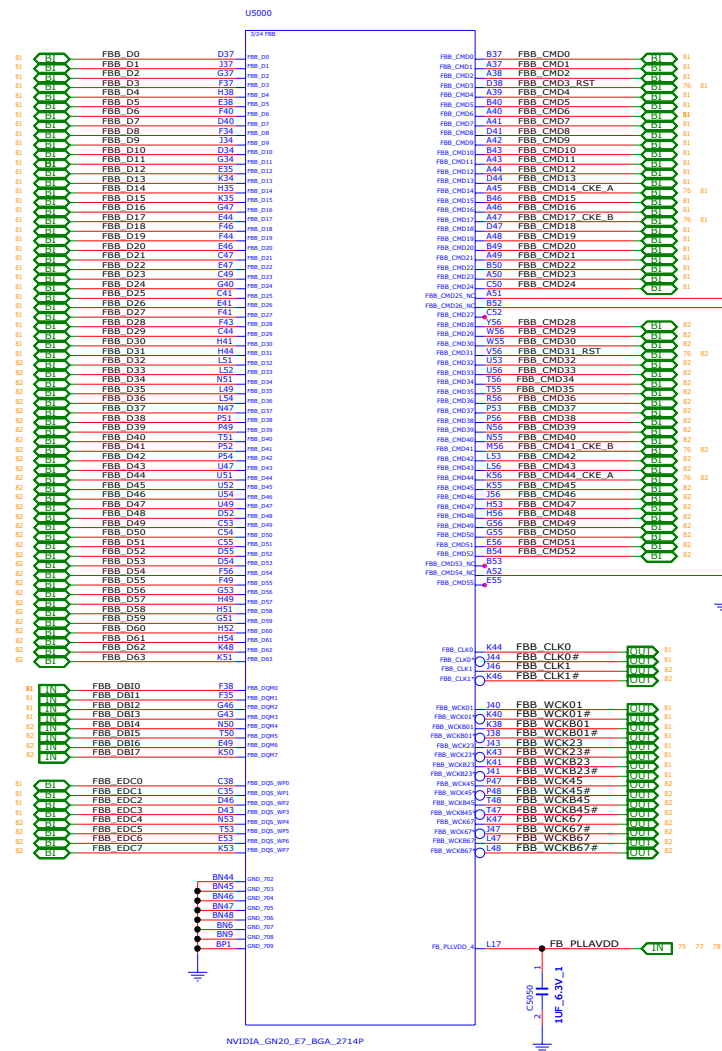
SHEET 75 of 119

PCB P/N	60xxxxxxxxxx	PCB VER.	XXX
---------	--------------	----------	-----

	2
--	---

GPU MEMORY PARTITION B

LOCATION NUMBER : 5000~5499



INVENTEC

MODEL PROJECT FUNCTION

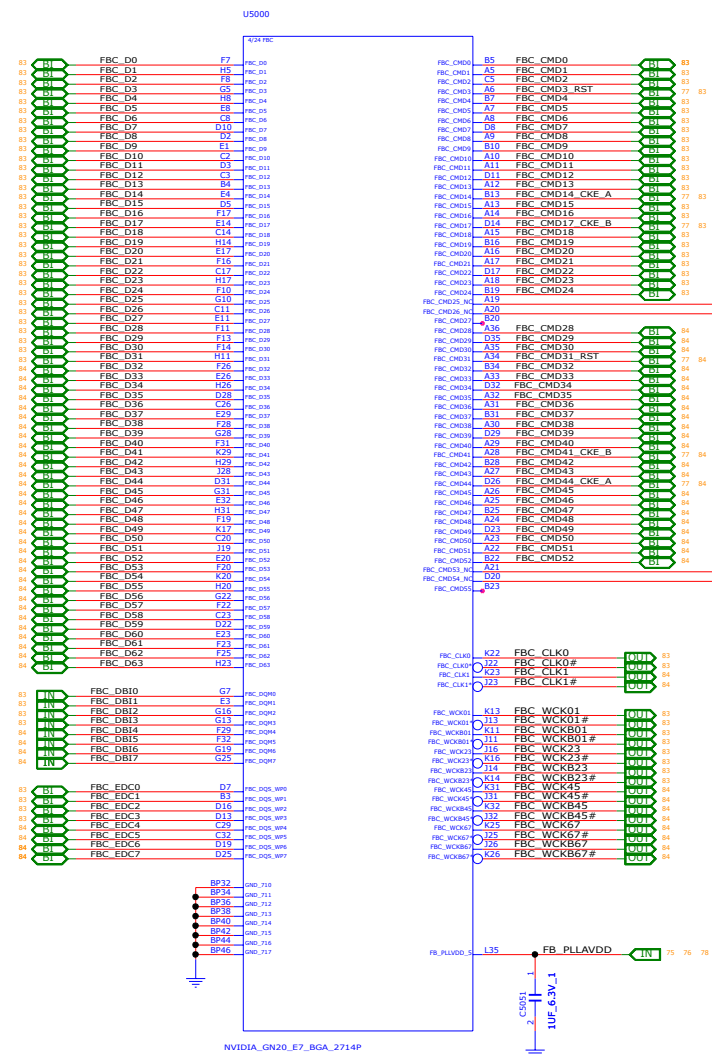
CODE CS 1310xxxx-0-0

REV X01

CHANGE BY	XXX	DATE	21-OCT-2002
PCB P/N	6Pxxxxxxxxxx	PCB VER	XXX
SHEET	76	of	116

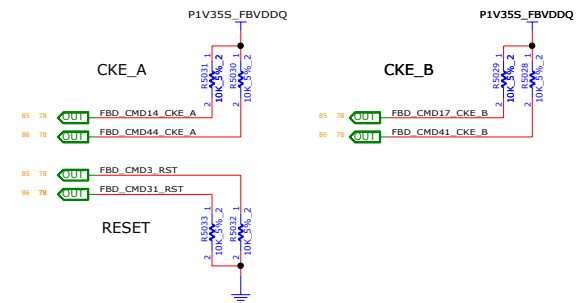
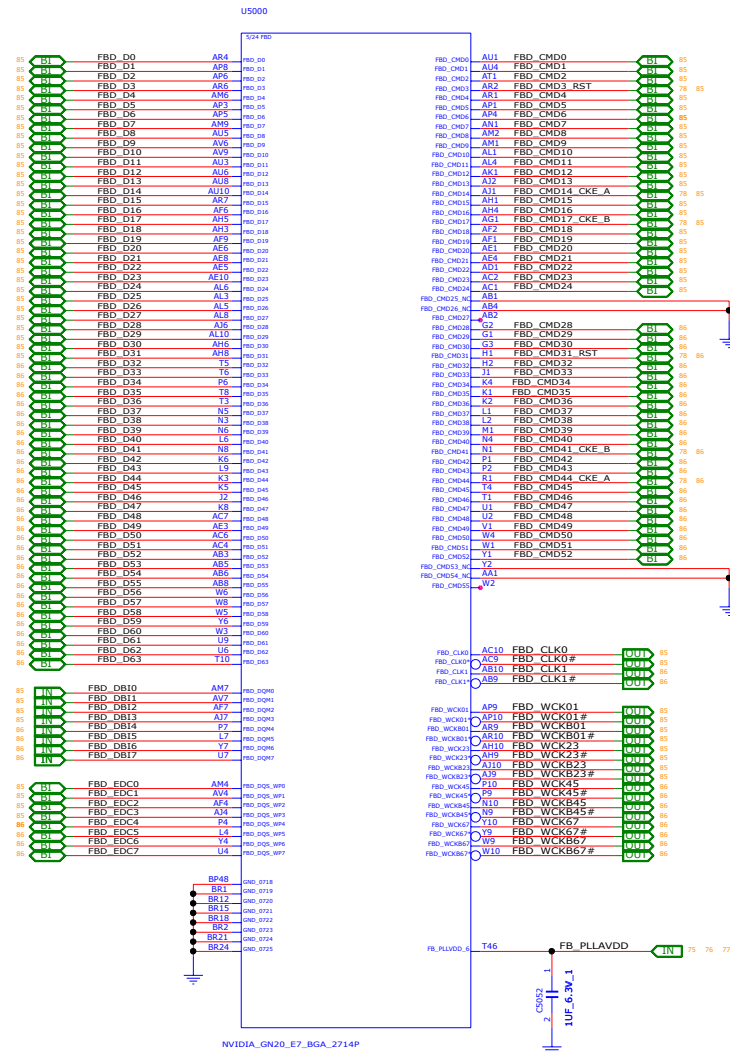
GPU MEMORY PARTITION C

LOCATION NUMBER : 5000~5499



GPU MEMORY PARTITION D

LOCATION NUMBER : 5000~5499

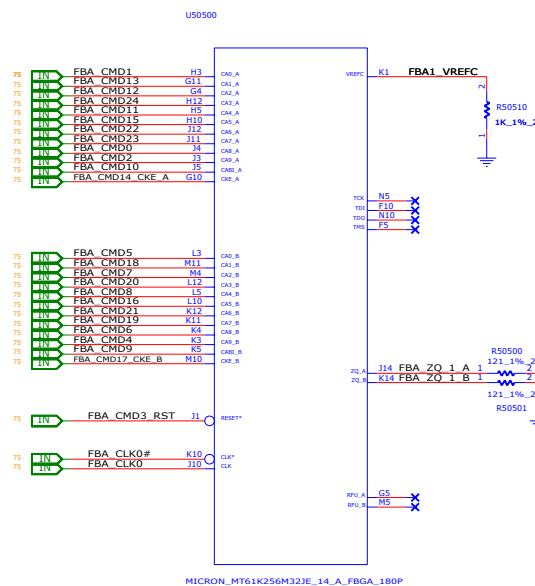
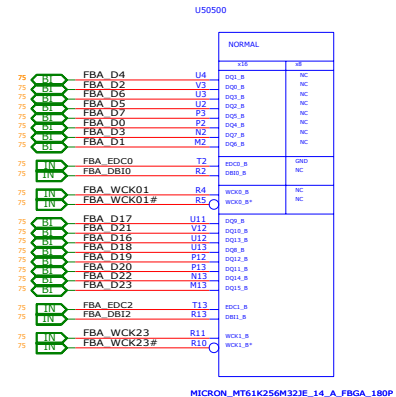
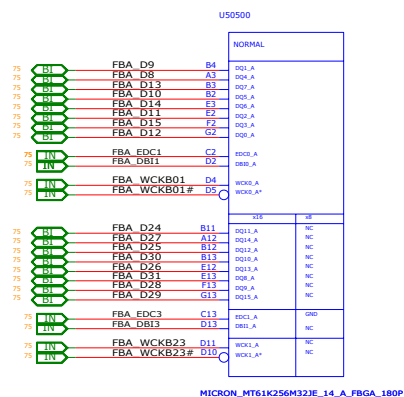
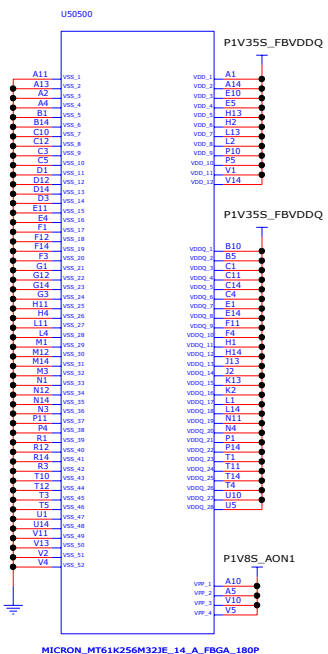


www.teknisi-indonesia.com

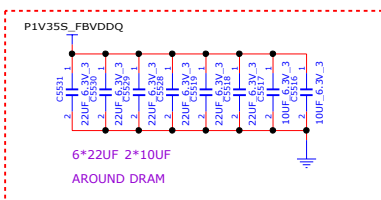
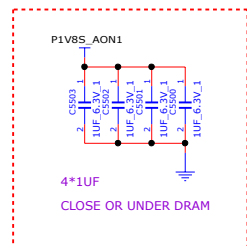
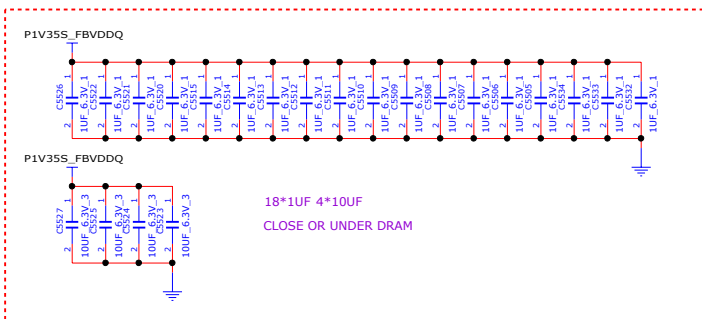
INVENTEC

GPU MEMORY FBA PARTITION 31-0

LOCATION NUMBER : 5500~5549



DECAP VIA : AT LEAST 2 GND VIAS AND 2 POWER VIAS FOR EACH CAP



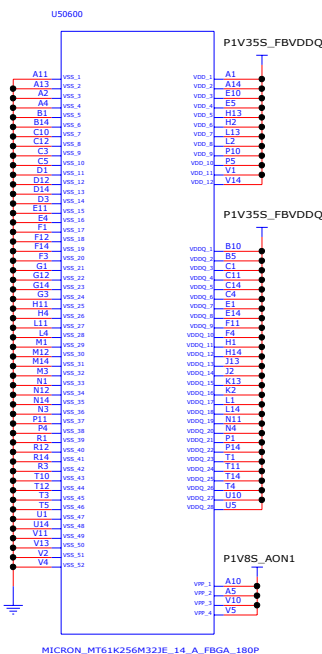
INVENTEC

TITLE		MODEL_PROJECT_FUNCTION		DOC NUMBER		REV	
Block		Diagram		1310xxxx-0-0		X01	
SIZE	A7	CODE	CS	SHEET	76	of	110

CHANGE BY	XXX	DATE	21-OCT-2002
PCB P/N	67xxxxxxx	PCB VER	XXX

GPU MEMORY FBA PARTITION 63-32

LOCATION NUMBER : 5550~5599

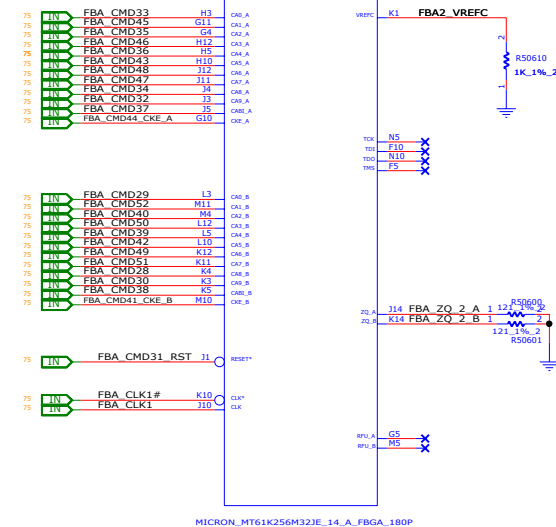


NORMAL			
FBA D41	B4	DQ1.A	
FBA D40	A3	DQ4.A	
FBA D39	B3	DQ1.A	
FBA D44	B2	DQ5.A	
FBA D47	C3	DQ6.A	
FBA D46	E2	DQ1.A	
FBA D43	F2	DQ2.A	
FBA D45	G2	DQ1.A	
FBA D37	M2	DQ1.A	
FBA EDC3	C2	EDC1.A	
FBA DB15	D2	DB1.A	
FBA WCKB45	D4	WCK1.A	
FBA WCKB45#	D5	WCK1.A	
FBA D60	B11	DQ1.A	
FBA D61	A12	DQ1.A	
FBA D62	B12	DQ1.A	
FBA D58	B13	DQ1.A	
FBA D63	E12	DQ1.A	
FBA D59	F13	DQ1.A	
FBA D57	F13	DQ1.A	
FBA D56	G13	DQ1.A	
FBA EDC7	C13	EDC1.A	
FBA DB17	D13	DB1.A	
FBA WCK67	D11	WCK1.A	
FBA WCK67#	D10	WCK1.A	

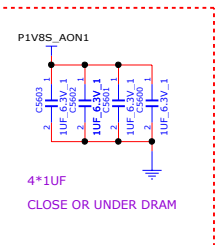
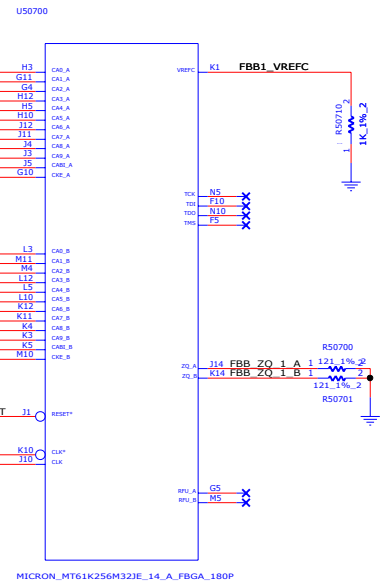
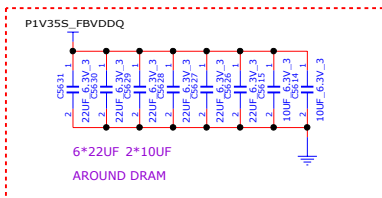
MICRON_MT61K256M32JE_14_A_FBGA_180P

NORMAL			
FBA D32	U4	DQ1.B	NC
FBA D33	V3	DQ1.B	NC
FBA D36	U3	DQ1.B	NC
FBA D39	U2	DQ1.B	NC
FBA D34	P3	DQ1.B	NC
FBA D38	P2	DQ1.B	NC
FBA D35	G2	DQ1.B	NC
FBA D37	M2	DQ1.B	NC
FBA EDC4	T2	EDC1.B	NC
FBA DB14	R2	DB1.B	NC
FBA WCK45	R4	WCK1.B	NC
FBA WCK45#	R5	WCK1.B	NC
FBA D55	U11	DQ1.B	NC
FBA D48	V12	DQ1.B	NC
FBA D53	U12	DQ1.B	NC
FBA D49	U13	DQ1.B	NC
FBA D54	P12	DQ1.B	NC
FBA D51	P13	DQ1.B	NC
FBA D52	N13	DQ1.B	NC
FBA D50	M13	DQ1.B	NC
FBA EDC6	T13	EDC1.B	NC
FBA DB16	R13	DB1.B	NC
FBA WCK67	R11	WCK1.B	NC
FBA WCK67#	R10	WCK1.B	NC

MICRON_MT61K256M32JE_14_A_FBGA_180P



LOCATION NUMBER : 5600~5649



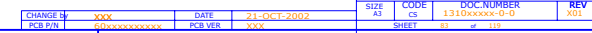
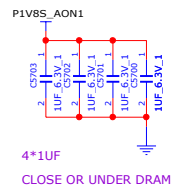
LOCATION NUMBER : 5650~5699



4*1UF

CLOSE OR UNDER DRAM

LOCATION NUMBER : 5700~5749



LOCATION NUMBER : 5750~5799

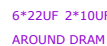


CHANGE BY	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	DOC. NUMBER	1310xxxxx-0-0	REV	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX			SHEET	84	of	119		

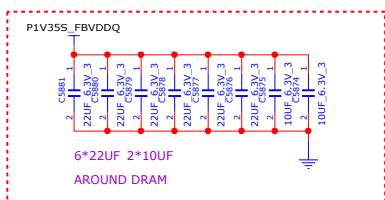
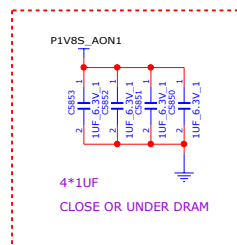
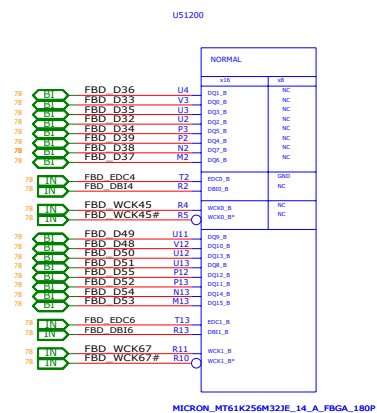
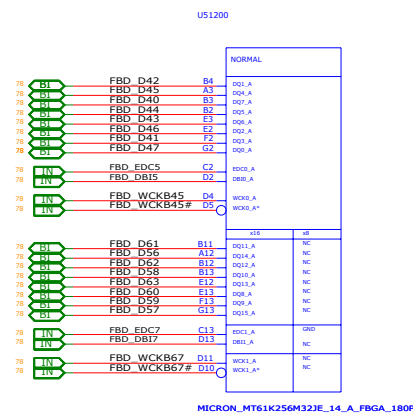
LOCATION NUMBER : 5800~5849



18*1UF 4*10UF
CLOSE OR UNDER DRAM

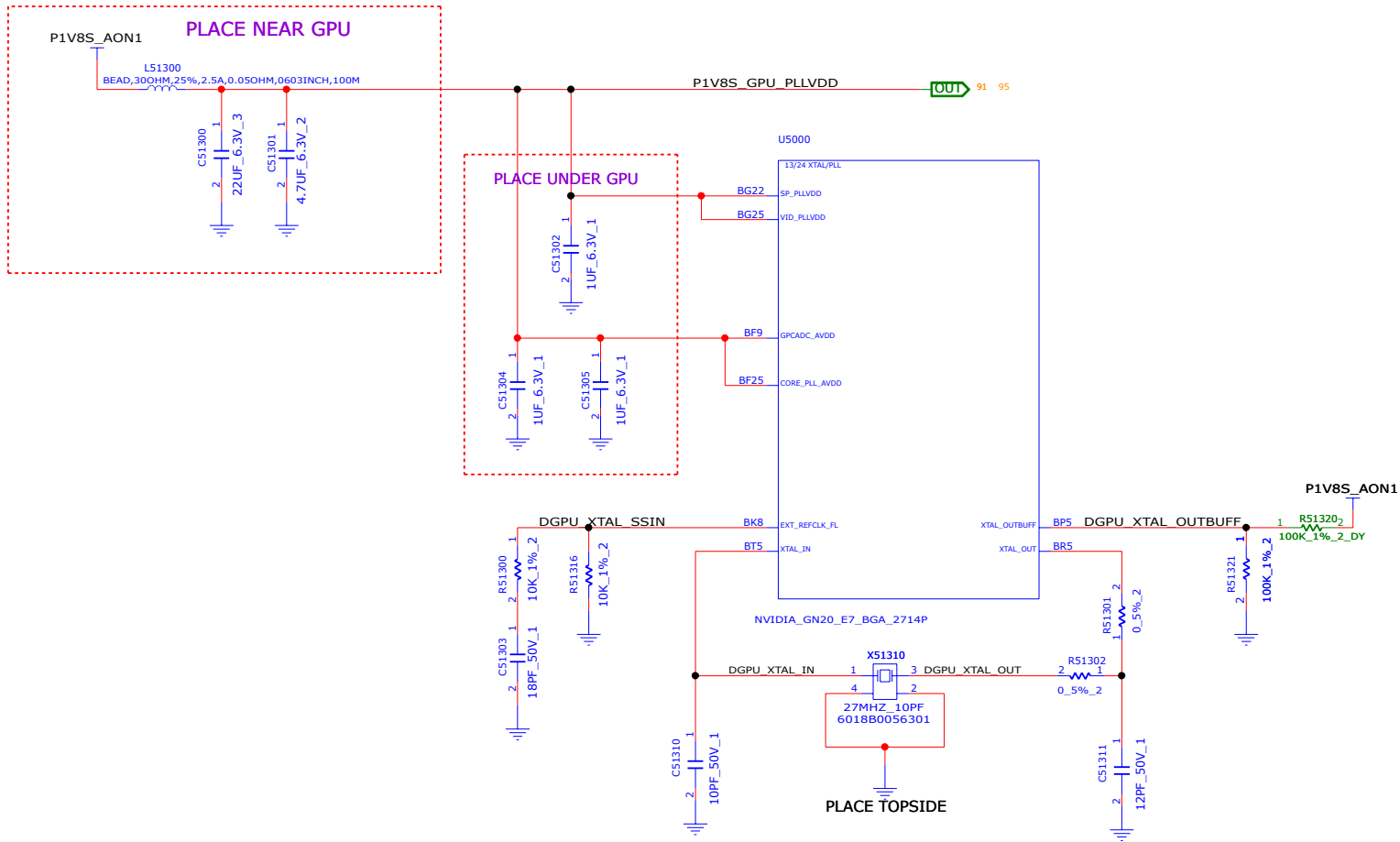


LOCATION NUMBER : 5850~5899



GPU 27 MHZ XTAL

LOCATION NUMBER : 5000~5499, 51300~51399



INVENTEC

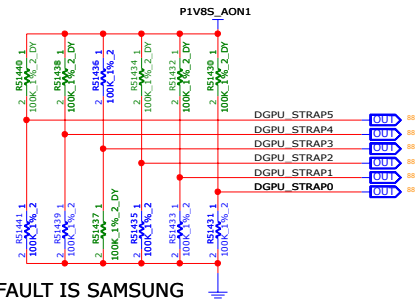
TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3 CODE CS
DOC. NUMBER 1310xxxx-0-0
REV X01

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX
SHEET	87 of 119		

GPU VBIOS, STRAPS

LOCATION NUMBER : 5000~5499, 51400~51499



DEFAULT IS SAMSUNG

SAMSUNG K4Z80325BC-HC14
6019B2086501
STRAP 0X0=000
MICRON MT61K256M32JE-14:A
6019B1847701
STRAP 0X1=001
SAMSUNG K4ZAF325BM-HC14
6019B2086601
STRAP 0X9=0M0
MICRON :R51430 STUFF
R51431 NOT STUFF

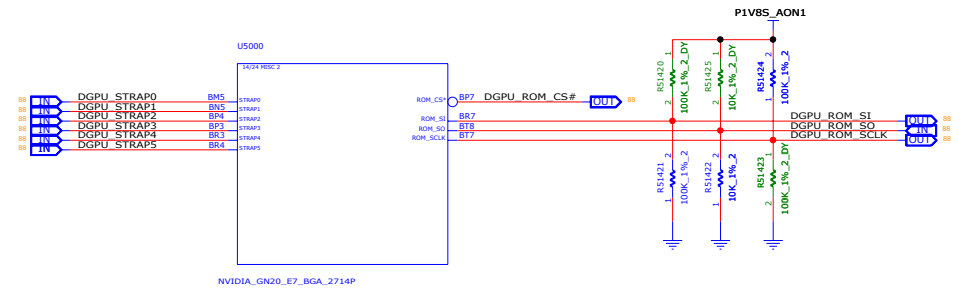
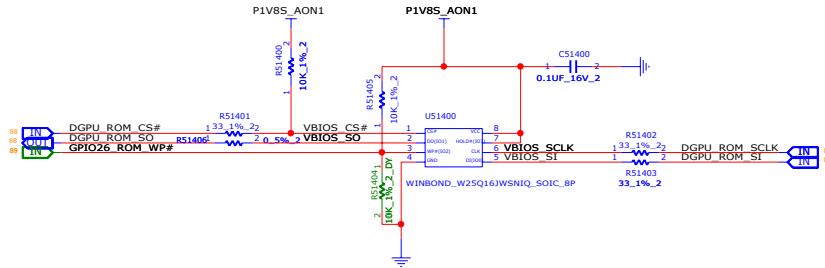


Table 9.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number (see Memory RVL for memory configs corresponding to these numbers)
STRAP2	STRAP1	STRAP0	
L	L	L	0 [0x0000]
L	L	H	1 [0x0001]
L	H	L	2 [0x0002]
L	H	H	3 [0x0003]
H	L	L	4 [0x0004]
H	L	H	5 [0x0005]
H	H	L	6 [0x0006]
H	H	H	7 [0x0007]
L	L	M	8 [0x0008]
L	M	L	9 [0x0009]
L	M	H	10 [0x000A]
L	H	M	11 [0x000B]
M	L	L	12 [0x000C]
M	L	H	13 [0x000D]
M	H	L	14 [0x000E]
M	H	H	15 [0x000F]

Strap Pins see Note			RAMCFG Setting Number (see Memory RVL for memory configs corresponding to these numbers)
STRAP2	STRAP1	STRAP0	
H	L	M	16 [0x0010]
H	M	L	17 [0x0011]
H	M	H	18 [0x0012]
H	H	M	19 [0x0013]
L	M	M	20 [0x0014]
M	L	M	21 [0x0015]
M	M	L	22 [0x0016]
M	M	H	23 [0x0017]
M	H	M	24 [0x0018]
H	M	M	25 [0x0019]
M	M	M	26 [0x001A]

Page29: MISC: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[10:0]		
L	L	L	00000	RAMCFG TBO	H=High :Tied to 1.8V
L	H	L	00010	RAMCFG TBO	M=Middle:Tied to 0.9V
L	H	H	00011	RAMCFG TBO	L=Low :Tied to 0V
H	H	L	00110	RAMCFG TBO	DEFAULT
L	L	H	00001	RAMCFG MICRON	

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0]FS_OVERT	1:ENABLE 0:DISABLE	
H	H	H	0111	FS_OVERT ENABLE	DEFAULT
H	H	M	0000	FS_OVERT DISABLE	

STRAPS	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	M	0	1	0	1
H	L	L	0	1	0	0
L	H	M	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

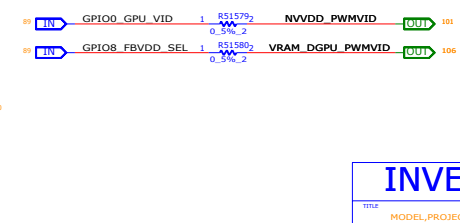
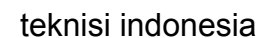
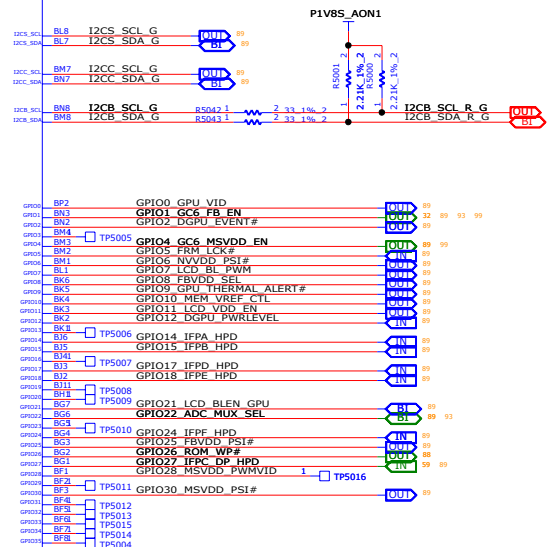
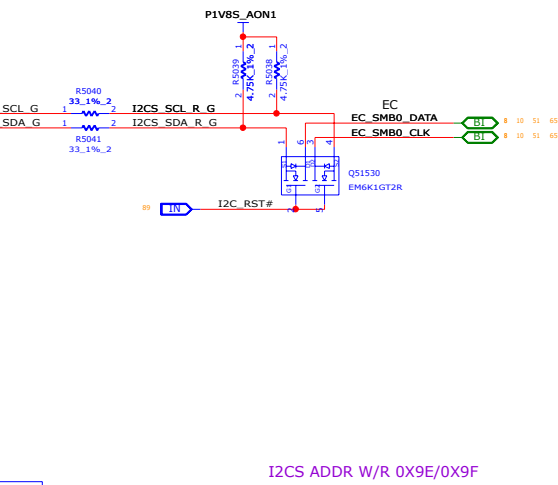
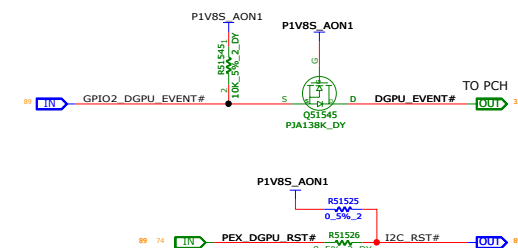
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL RESBRAND
0:DEVID_SEL ORIGINAL
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Default

INVENTEC

MODEL_PROJECT,FUNCTION		DOC NUMBER		REV
Block	Diagram	CS	SI	
CHANG	BY	XXX	DATE	21-OCT-2002
PCB P/N	XXXXXXXXXXXX	PCB VER	XXX	
SHEET	88	of	118	X01

LOCATION NUMBER : 5000~5499, 51500~51599

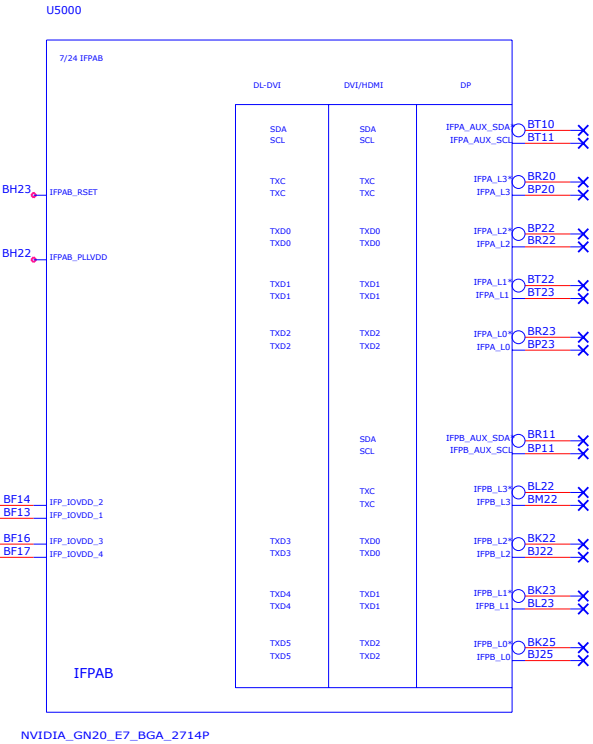


INVENTEC

				TITLE MODEL,PROJECT,FUNCTION Block Diagram			
CHANGE #	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET 89 of 110			

GPU IFP_AB

LOCATION NUMBER : 5000~5499, 51800~51899



INVENTEC

TITLE

MODEL,PROJECT,FUNCTION
Block / Diagram

SIZE
A3

CODE
CS

DOC.NUMBER
1310xxxx-0-0

REV
X01

CHANGE by
PCB P/N

XXX
60xxxxxxxxxx

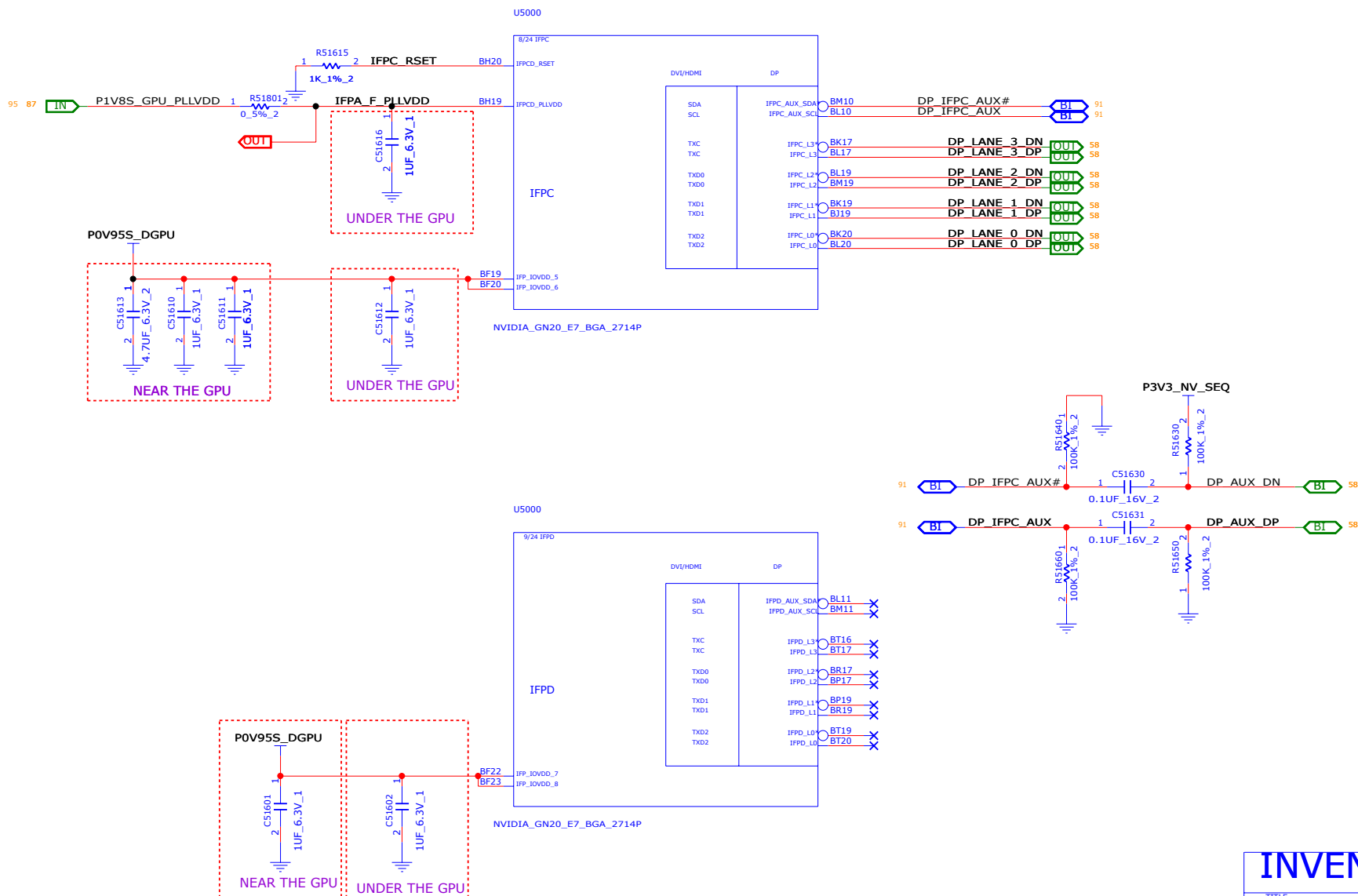
DATE
PCB VER

21-OCT-2002
XXX

SHEET
90 of 119

GPU IFP_CD(DP)

LOCATION NUMBER : 5000~5499, 51600~51699



INVENTEC

TITLE

MODEL,PROJECT,FUNCTION

Block Diagram

DOC.NUMBER

1310xxxx-0-0

REV

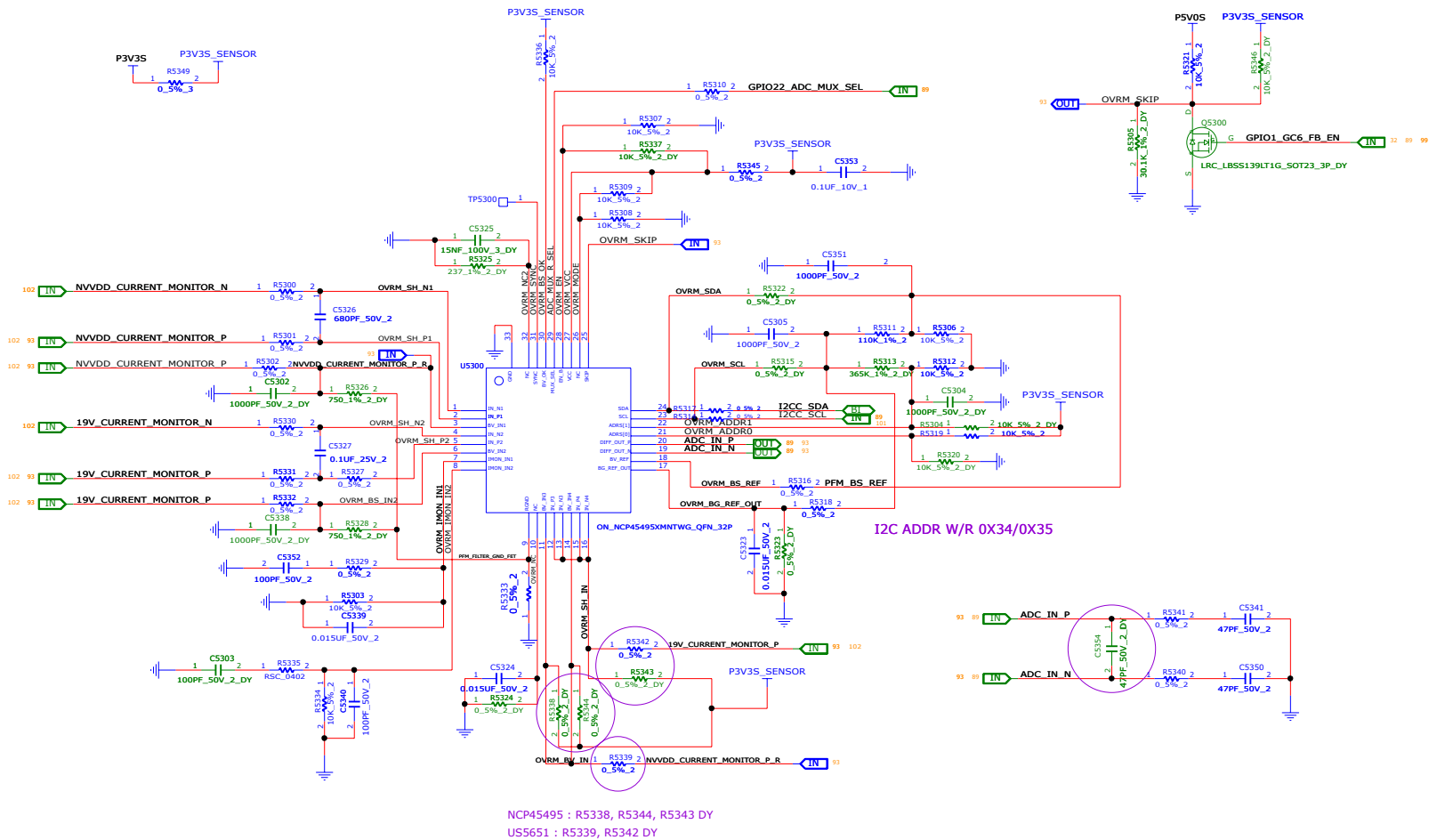
X01

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SHEET	91 of 119
-------	-----------

OVR-M NCP45495 & US5651(COALY)

LOCATION NUMBER : 5300~5399(NCP45495)



INVENTEC

TITLE		MODEL PROJECT FUNCTION		DOC NUMBER		REV	
Block		Diagram		1310xxxx-0-0		X01	
SIZE	A7	CODE	CS	SHEET	31	of	110

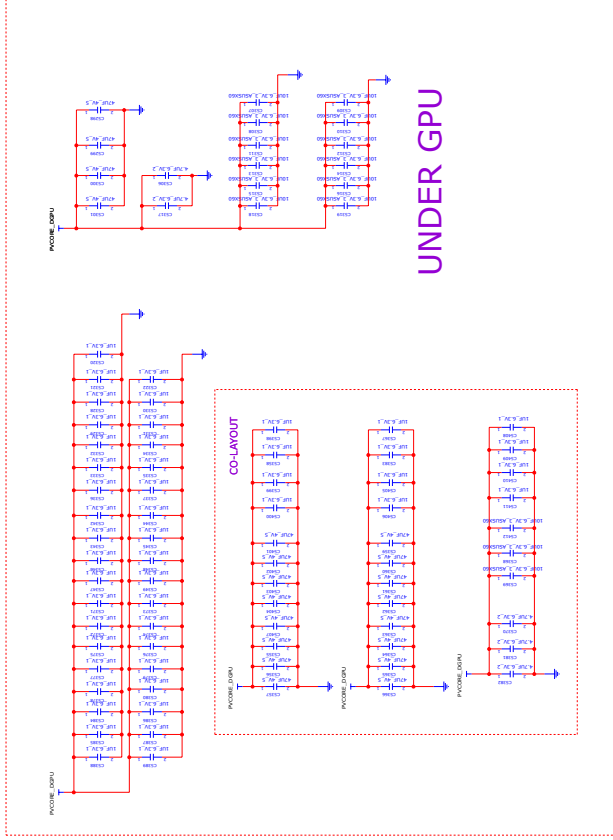
CHANGE BY	XXX	DATE	21-OCT-2002
PCB P/N	6Pxxxxxxxxxx	PCB VER	XXX

LOCATION NUMBER : 5000~5499



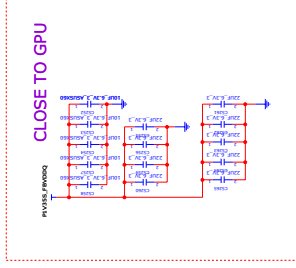
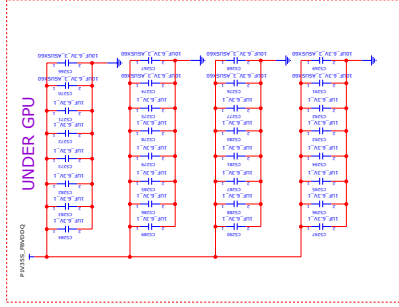
GPU NVVDD DECOUPLING

LOCKDOWN NUMBER: 1500-0099



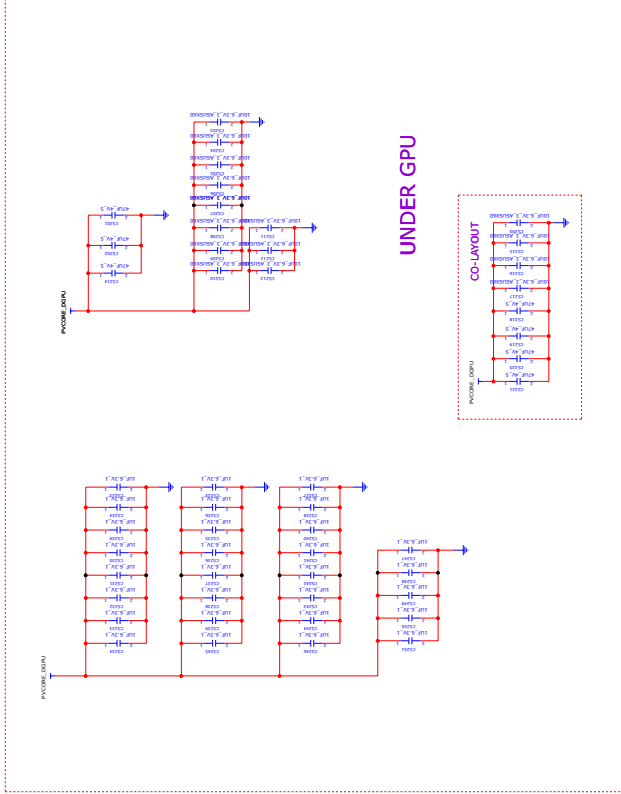
GPU FBVDDQ DECOUPLING

LOCATION NUMBER : 5000 ~ 5499

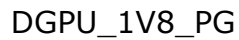


GPU MSVDD DECOUPLING

LOCATION NUMBER: 1000-5949



LOCATION NUMBER : 5900~5999



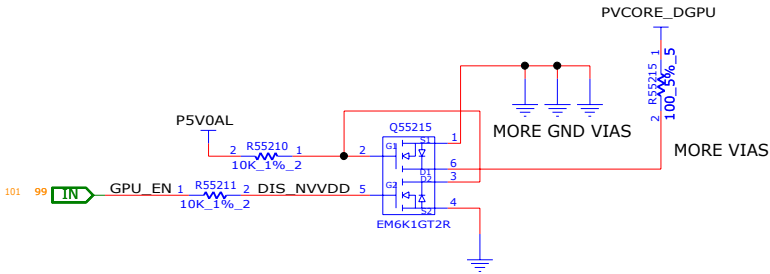
INVENTEC

				TITLE MODEL,PROJECT,FUNCTION Block Diagram			
CHANGE BY	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	DOC NUMBER 1310XXXXX-0-0	REV X01
PCB P/N	60XXXXXXXX	PCB VER	XXX	SHEET 89 of 119			

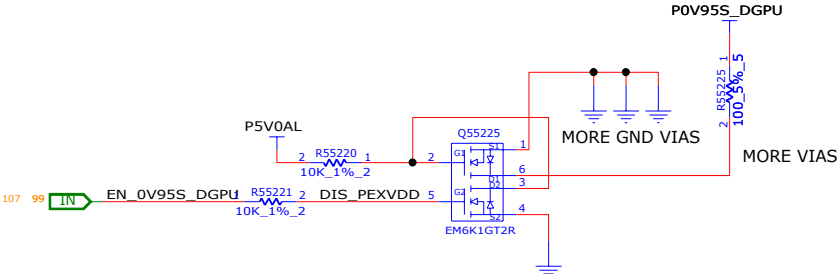
GPU POWER DISCHARGE

LOCATION NUMBER : 55200~55299

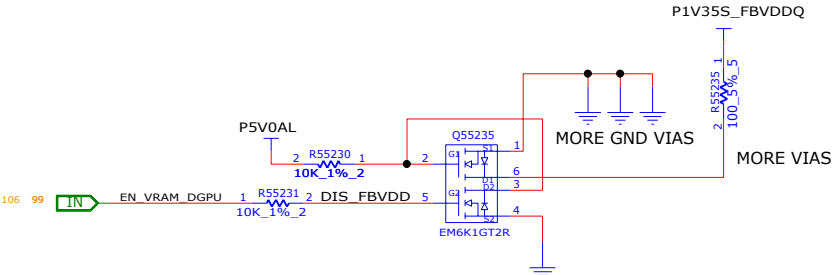
NVVD DISCHARGE



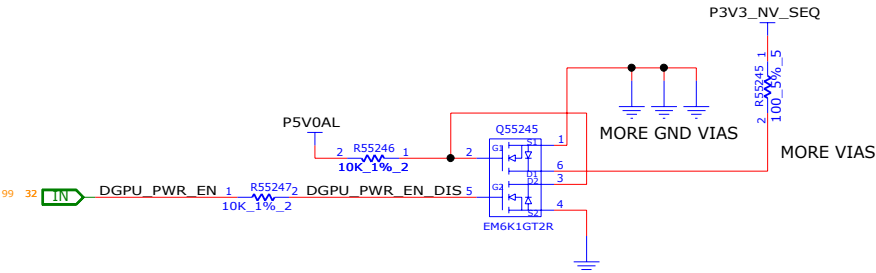
PEXVDD DISCHARGE



FBVDD DISCHARGE



P3V3_NV_SEQ DISCHARGE



INVENTEC

TITLE

MODEL, PROJECT, FUNCTION

Block Diagram

SIZE A3 CODE CS

SHEET 100 of 119

DOC. NUMBER 1310xxxx-0-0

REV X01

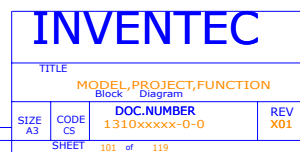
CHANGE by XXX

PCB P/N 60xxxxxxxxxx

DATE 21-OCT-2002

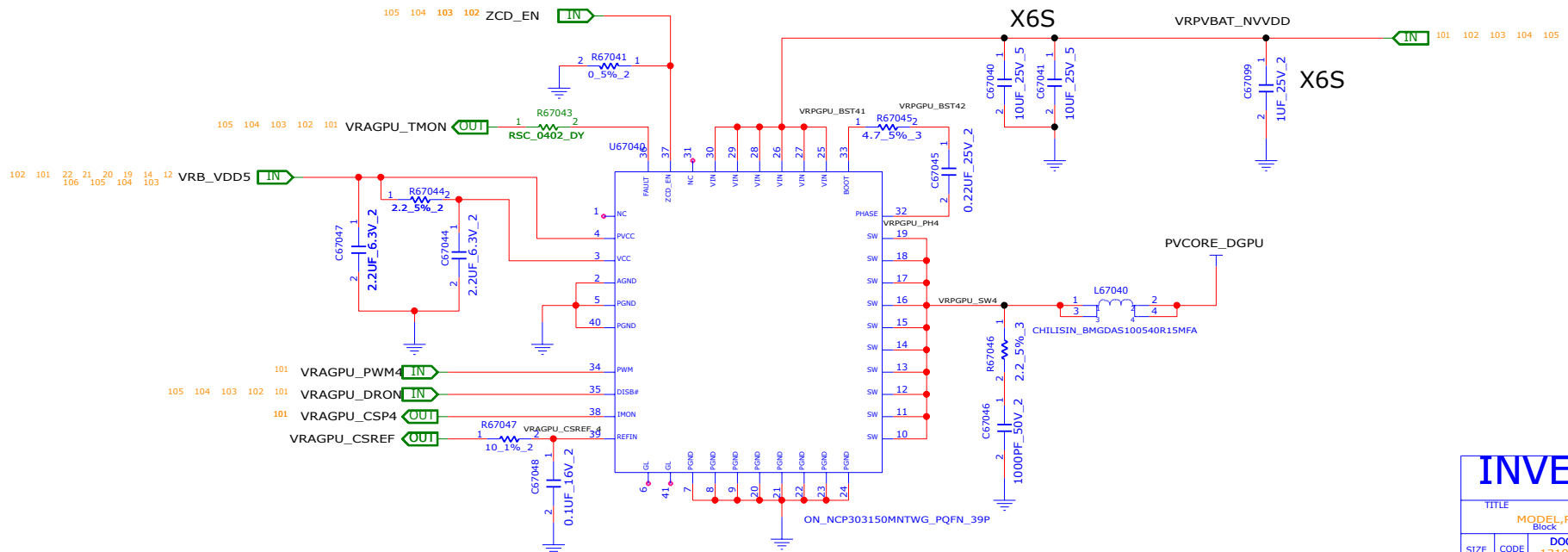
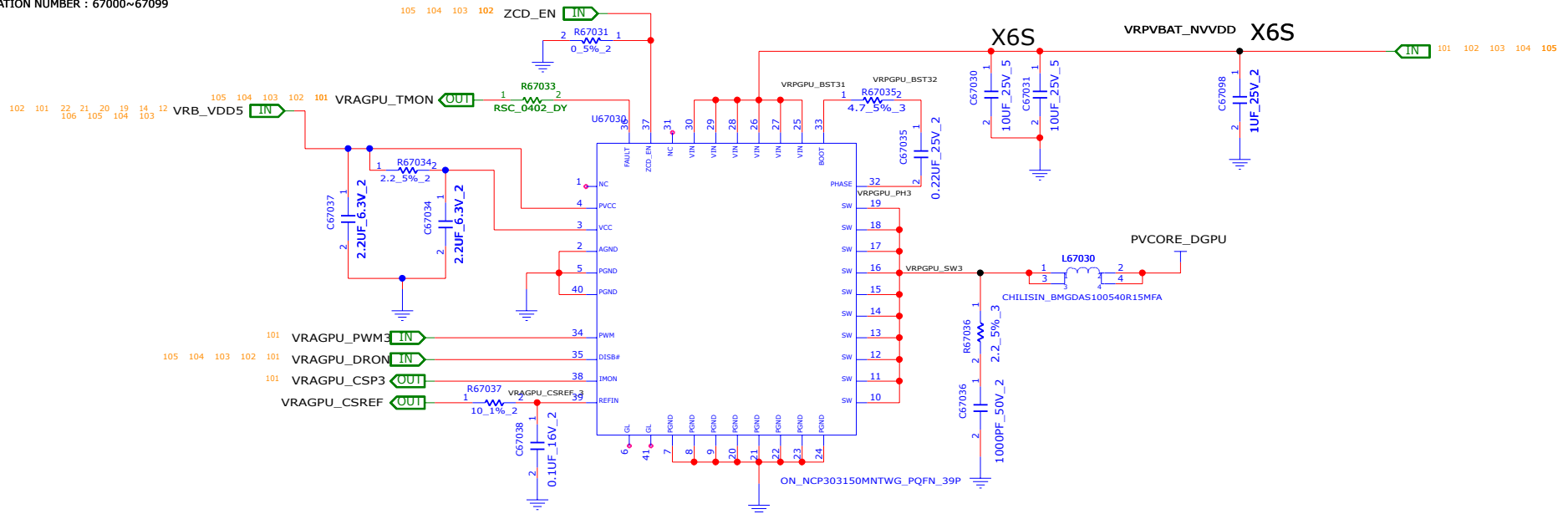
PCB VER XXX

LOCATION NUMBER : 67000~67099



PVCORE_DGPU (NCP303150_3-4P)

LOCATION NUMBER : 67000~67099



INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
DOC. NUMBER			
1310xxxx-0-0			
REV			
X01			

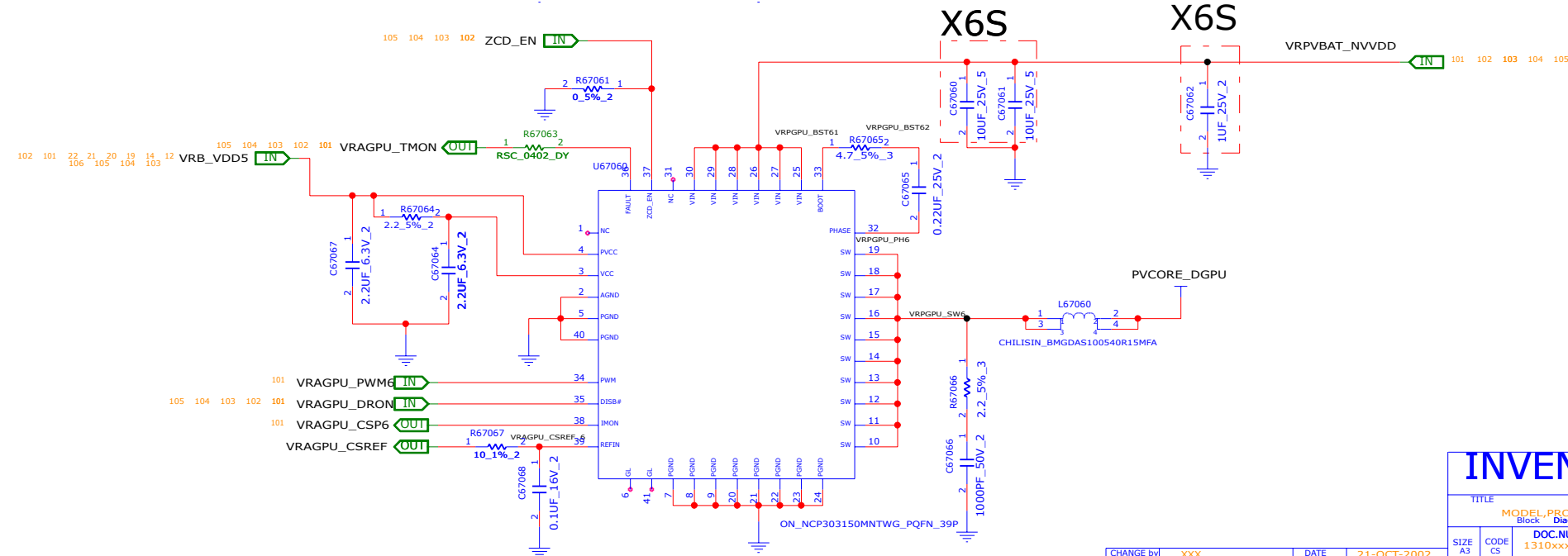
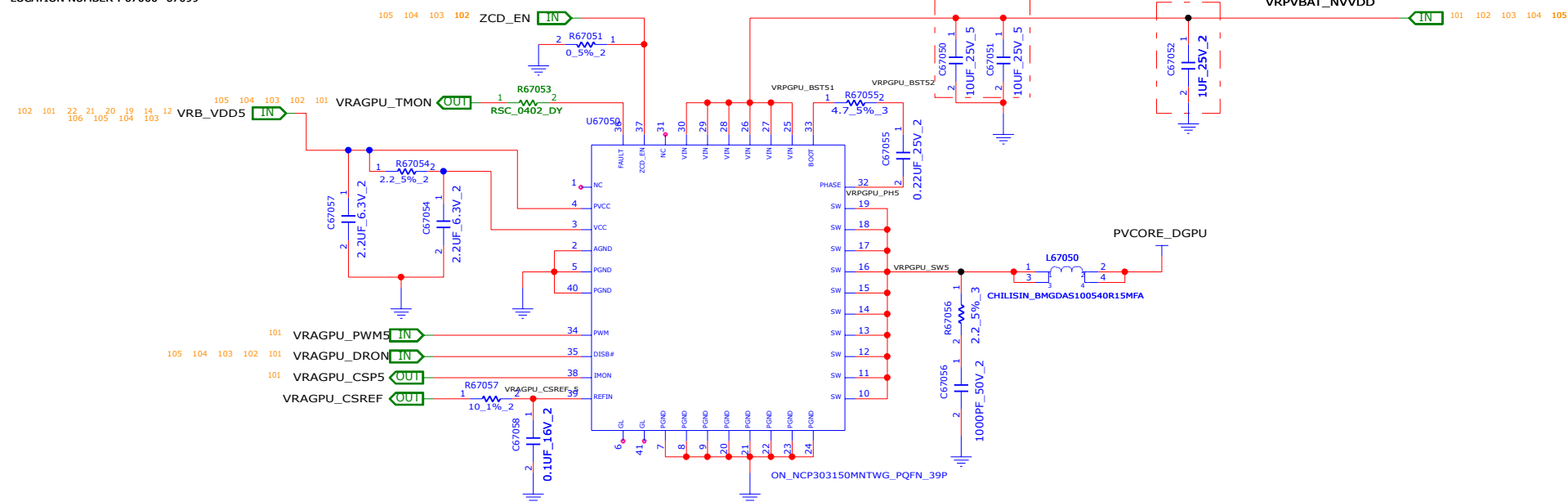
CHANGE by	XXX
PCB P/N	60xxxxxxxxxx

DATE	21-OCT-2002
PCB VER	XXX

SHEET	103 of 119
-------	------------

PVCORE_DGPU (NCP303150_5-6P)

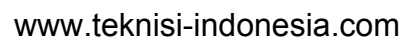
LOCATION NUMBER : 67000~67099



INVENTEC

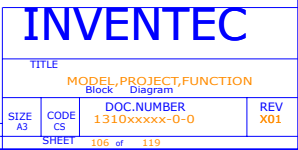
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		104 of 119	

LOCATION NUMBER : 67000~67099



X01	
-----	--

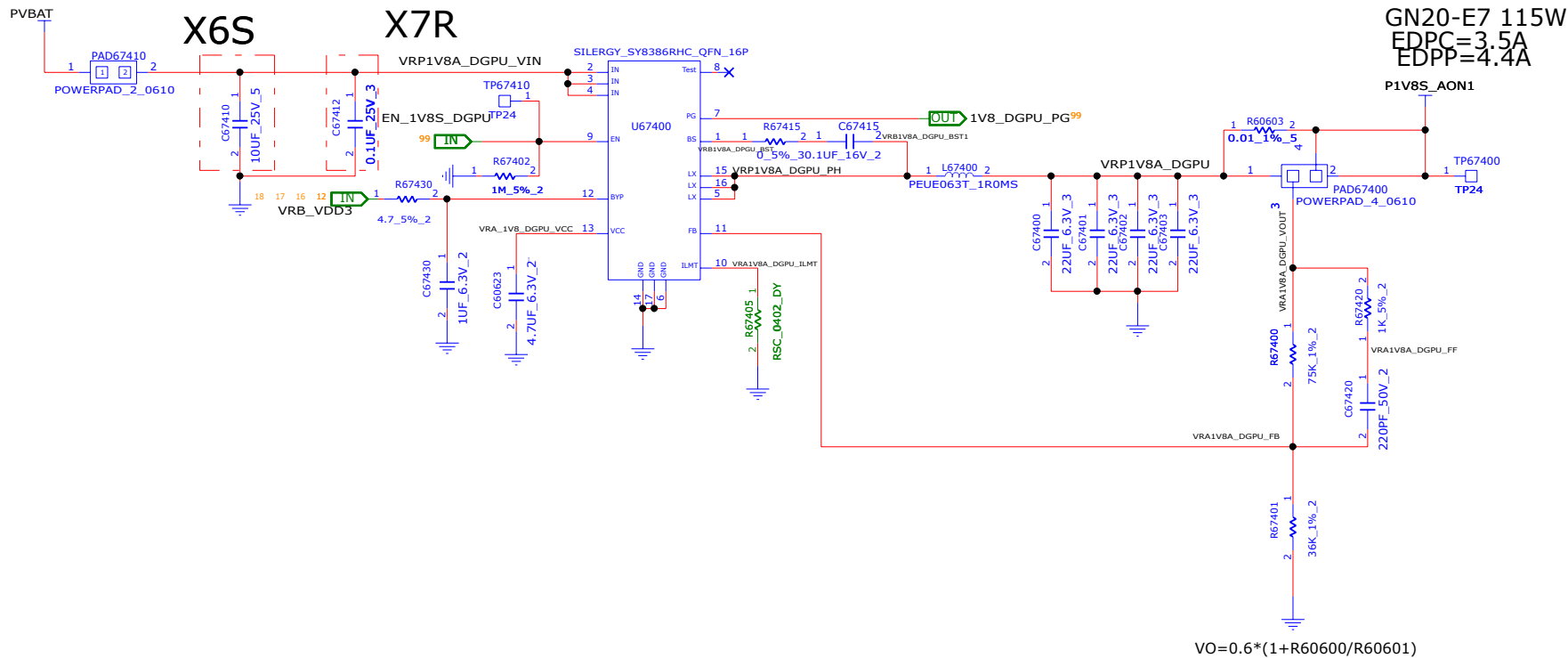
LOCATION NUMBER : 67200~67299



07e409180c100f00520f7a8d74001513

P1V8S_AON1 (SY8386)

LOCATION NUMBER : 67400~67499



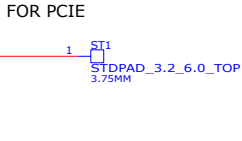
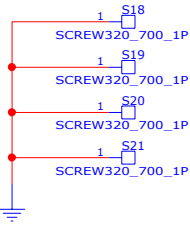
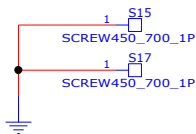
INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET	108 of 119		

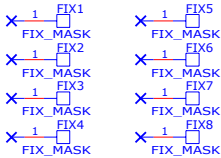
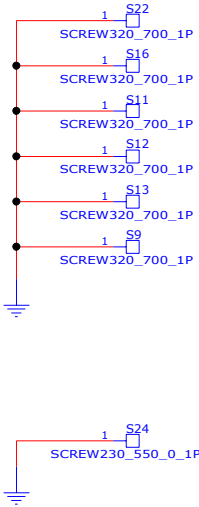
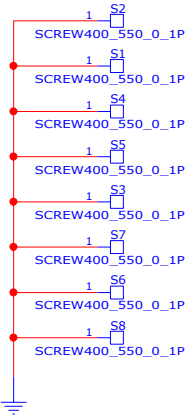
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

PCB SCREW / MASK / STANDOFF

LOCATION NUMBER : 0~49



GPU CPU



INVENTEC

TITLE
MODEL PROJECT.FUNCTION
XDP & RE CONNL

SIZE A3 CODE CS DOC.NUMBER 1310xxxxx-0-0 REV X01

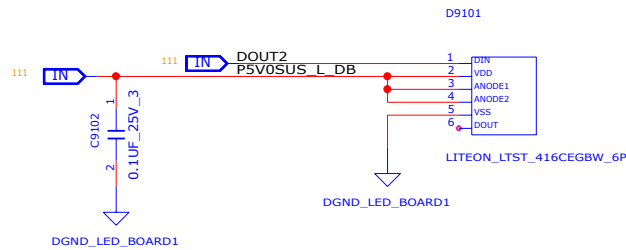
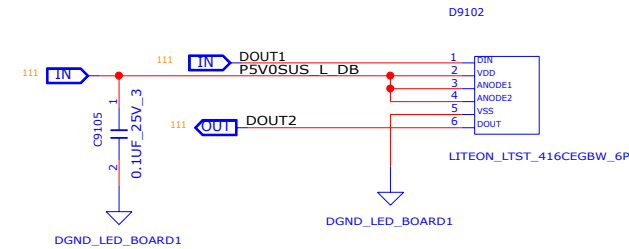
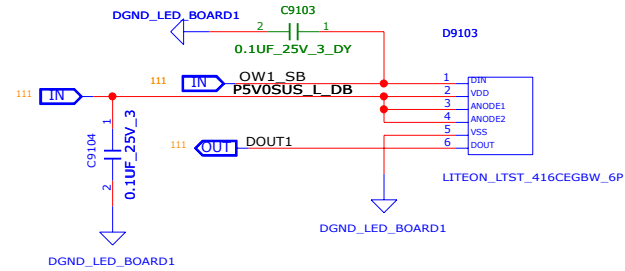
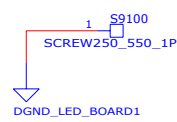
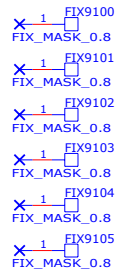
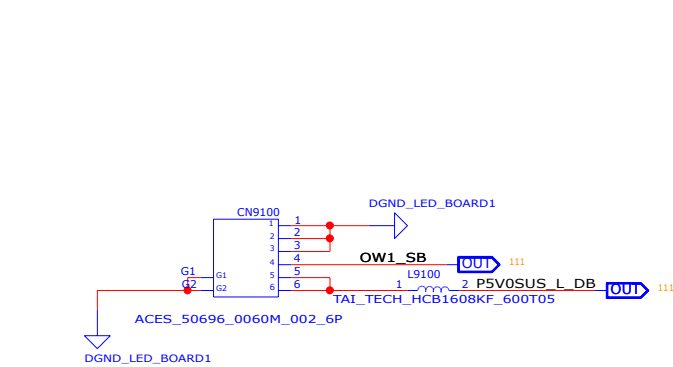
CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxx PCB VER XXX

SHEET 109 of 119

8	7	6	5	4	3	2	1
DB BOARD							
PAGE110-118							
INVENTEC							
TITLE							
MODEL, PROJECT, FUNCTION							
Block / Diagram							
CHANGE by		DATE		SIZE		CODE	
PCB P/N		PCB VER		A3		CS	
XXX		21-OCT-2002		XXX		1310xxxx-0-0	
60xxxxxxxxxx		XXX		SHEET		110 of 119	
8	7	6	5	4	3	2	1

L-U-BAR BOARD

LOCATION NUMBER : 9100~9124



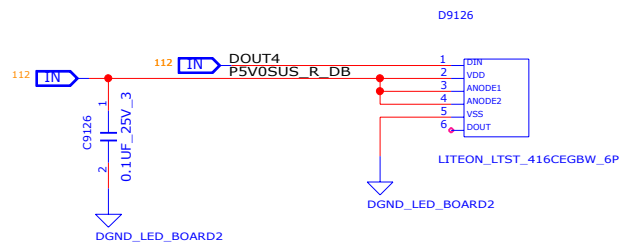
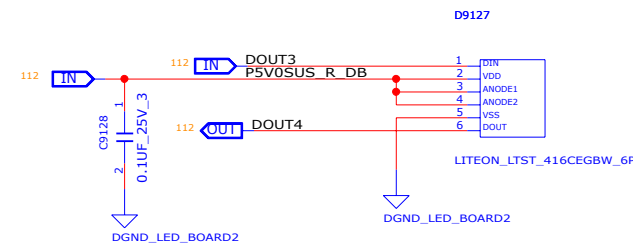
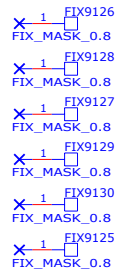
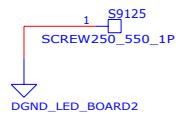
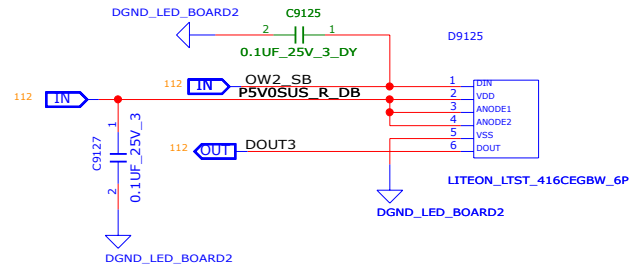
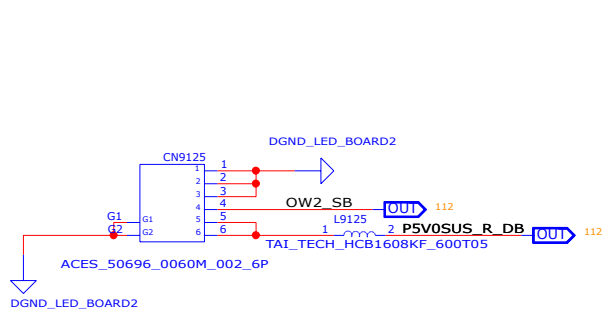
INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 111 of 119			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

R-U-BAR BOARD

LOCATION NUMBER : 9125~9149



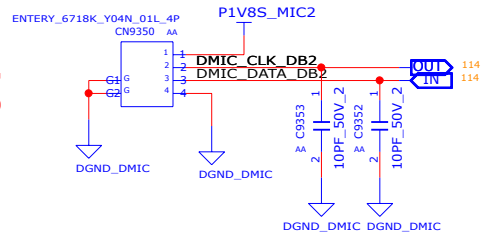
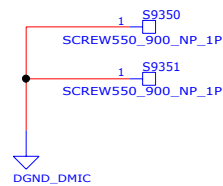
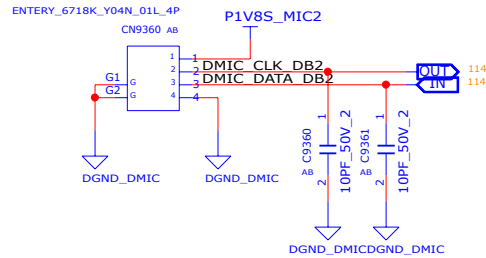
INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 112 of 119			

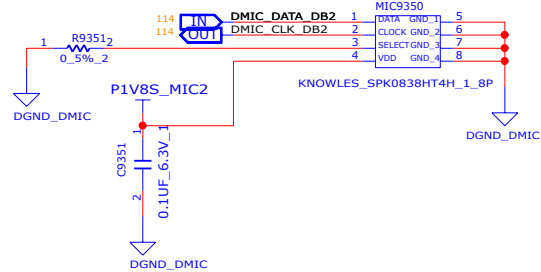
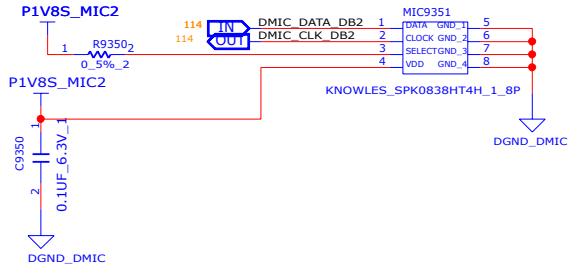
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

DMIC BOARD

LOCATION NUMBER : 9350~9399

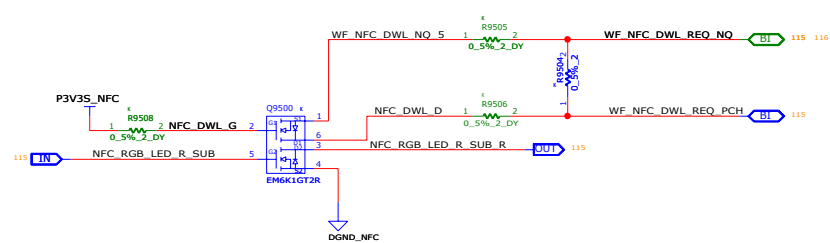
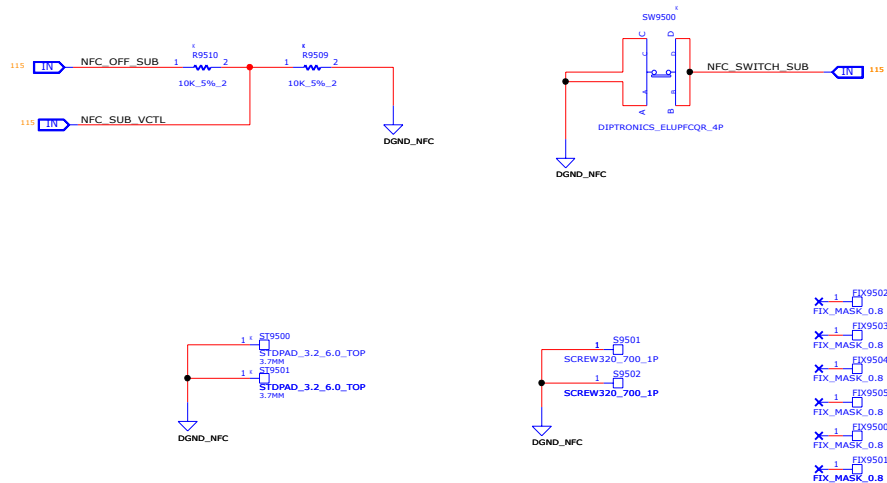
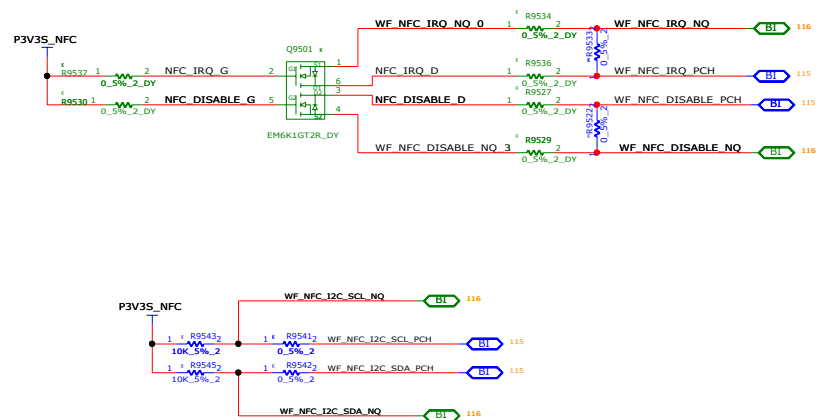
G5**G7**

- X 1 FIX9355
- FIX_MASK_0.8
- X 1 FIX9350
- FIX_MASK_0.8
- X 1 FIX9351
- FIX_MASK_0.8
- X 1 FIX9352
- FIX_MASK_0.8
- X 1 FIX9353
- FIX_MASK_0.8
- X 1 FIX9354
- FIX_MASK_0.8

**INVENTEC**TITLE
MODEL,PROJECT,FUNCTION
Block DiagramDOC.NUMBER
1310xxxx-0-0REV
X01

CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	SHEET	114 of 119
PCB P/N	60xxxxxxxxxx	PCB VER	XXX						

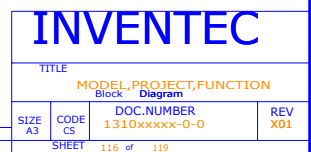
LOCATION NUMBER : 9500~9599

[illegible][illegible]

TITLE			
MODEL,PROJECT,FUNCTION RING LED			
SIZE A3	CODE CS	DOC. NUMBER 1310xxxxxx-0-0	REV X01
SHEET		115	of 119

CHANGE BY	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	DOC. NUMBER	1310XXXXX-0-0	REV	X01
PCB P/N	60XXXXXXXXXX	PCB VER	XXX	SHEET		115	of	119			

LOCATION NUMBER : 9500~9599

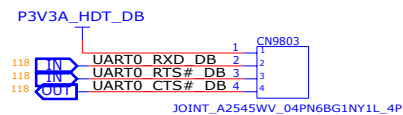
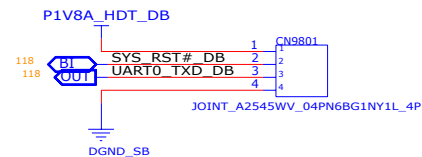
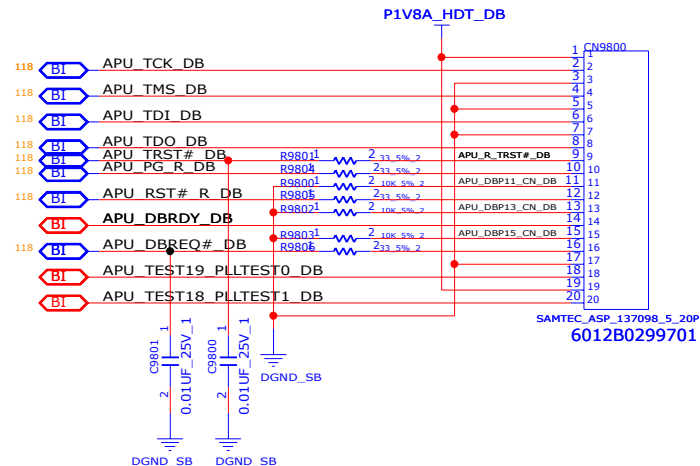
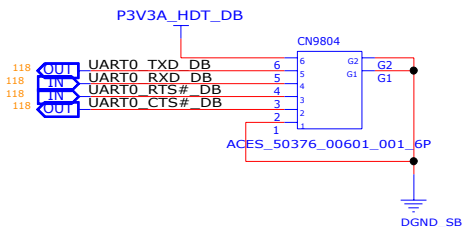
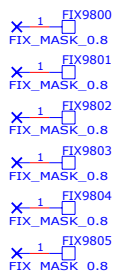
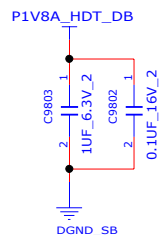
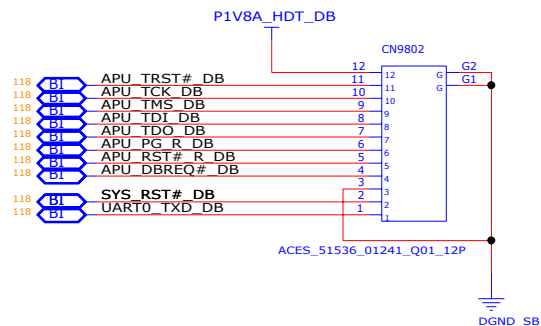


A



HDT DEBUG

LOCATION NUMBER : 9800~9849

**INVENTEC**

TITLE			
Block Diagram			
MODEL	PROJECT	FUNCTION	REV
1310xxxxx-0-0	1310xxxxx-0-0	1310xxxxx-0-0	X01
SIZE	CODE	SHEET	
A3	CS	118 of 119	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

D

C

B

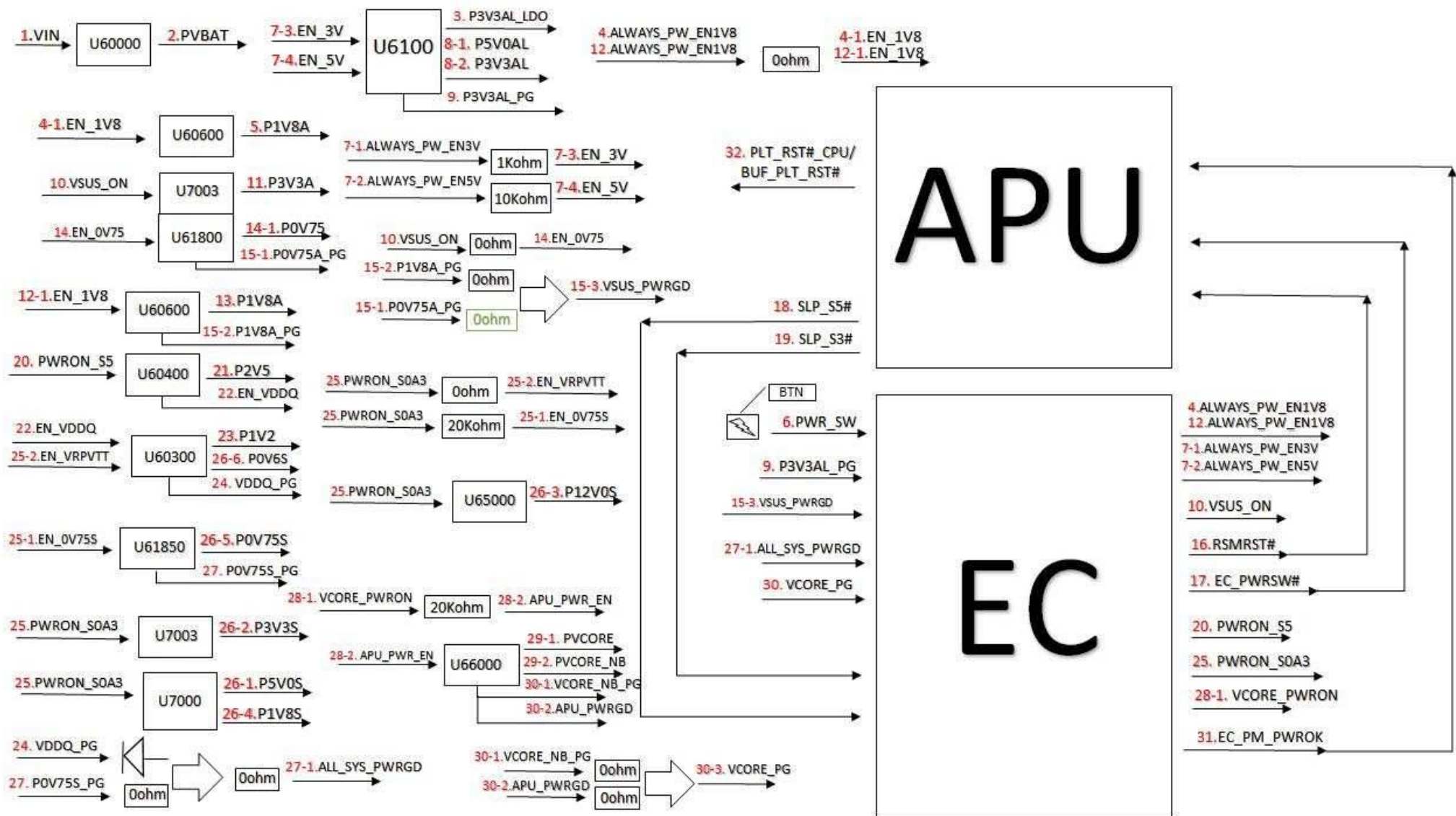
A

D

C

B

A



INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE		DOC. NUMBER	
A3		1310xxxx-0-0	
CODE		REV	
CS		X01	
SHEET		119 of 119	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX